Output impedance simulations for several RF power amplifiers.

First published: 9-june-2010, Wim Telkamp, PA3DJS.
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Why?

Reason for these simulations are the ongoing discussions about large signal output impedance of power amplifiers in the *"what happens to reflected energy?"* thread in *rec.radio.amateur.antenna*, around June 2010. Different opinions resulted in divergence rather than convergence.

To know something about the output impedance, can be of importance when reflections arrive at the amplifier.

Under maximum power transfer matching (with constant input drive and power supply conditions), there is a conjugated match (ZL = Zout*, "*" means conjugated value). Practically this means matching a load to an amplifier to obtain maximum output power (under non-varying drive). This also results in maximum gain. Of course after matching, variable capacitors should not be at maximum or minimum value. The conjugated match condition is not disputed here.

Many amplifiers are not operated under this condition:

1. Amplifier is driven below or above the settings used for maximum power match. A linear amplifier for envelope modulation schemes (SSB, AM, QAM, etc) is most of the time operated below best match conditions.
2. Several amplifiers have poor efficiency under matching for maximum power condition. Change matching towards lower power consumption reduces output power somewhat, but increases efficiency (I have learned that from PA0AKS).
3. Many (solid) state amplifiers have fixed match (for example: 2..30 MHz push-pull), and are used at varying power level, so will unlikely operate under conjugated matched condition.
4. Saturated mode or switched mode high efficiency designs are driven below maximum gain. When adjusted to maximum output power, devices will be destroyed (if no protection is present).

Why simulations instead of actual measurements? Everyone having a circuit simulator can reproduce the results and can change things to fulfill his own requirements. There will be no discussion on measurements (but maybe on device models); you can look to your own simulations. All simulations in this document were carried out with Beige Bag B^2 Spice A/D Professional, version 4.

7 circuits with increasing complexity were evaluated. Note that these circuits are for simulation only (as several components are left out) for simplicity.

Common Grid circuit with simple tank circuit.

This circuit has low component count and you can vary the plate load easily by changing the tuning capacitor and load resistor. As the output impedance is almost real (after correct tuning), one can use resistive load change to determine Zout.

Common Cathode circuit with simple tank circuit

Tuning this circuit is somewhat more complicated as there is some effect of the feedback capacitance. Plate current is no longer in (opposite) phase with plate voltage (for conjugated match tuning). It is expected that when you change the input circuit, Zout under reduced drive will change also.

"Class C" mosfet output stage

Actually this isn't a real class C stage, but a non-optimally tuned class E stage. Output impedance is no longer real, so you cannot use resistive load change, unless you extend with coaxial cable to make the impedance real. Here small signal injection is used to determine output VSWR. Also load pulling (taking phase into account) is used.

Circuit is added to show that reasonable efficiency may result in bad output VSWR and to show the influence of supply chokes on transient response of the amplifier.

Class AB LD mosfet output stage, single ended, 145 MHz.

Tuning is based on the on-chip drain and source voltages and charge carrier current through the device, without looking to output impedance. Load pulling is used to determine output impedance. Difference frequency is used to compare with load pulling. As the amplifier doesn't saturate, results should be similar.

A real class C Common Cathode output stage.

Voltage drive is used to reduce the time to do the simulation and conjugated match condition is close to maximum efficiency condition. It is added to show that you can have >50% efficiency under conjugated match condition, but highest efficiency doesn't require conjugated match.

Class AB Common Cathode circuit with Pi-filter matching.

This is the most elaborate circuit, but is closest to a real valve circuit. As changing the plate capacitor does also change the real component presented to the load, finding correct capacitor settings for the conjugated match condition is very difficult. When starting from scratch, you may require a full day.

Also here, output impedance under reduced drive may be dependent on input circuitry. As it is expected that the output impedance under reduces drive and/or mismatch will be complex, small signal injection method is used to determine output VSWR.

Class AB Common Cathode circuit with Pi-filter matching, reduced power and carefully selected drive impedance.

This simulation deviates from all others due the combination of output power and drive impedance in combination with the feedback capacitance from the valve. Output impedance remains reasonably 50 Ohms under changing load and drive level. Tuning of this circuit (in simulation) is easier as you stay away from (deep) saturation.

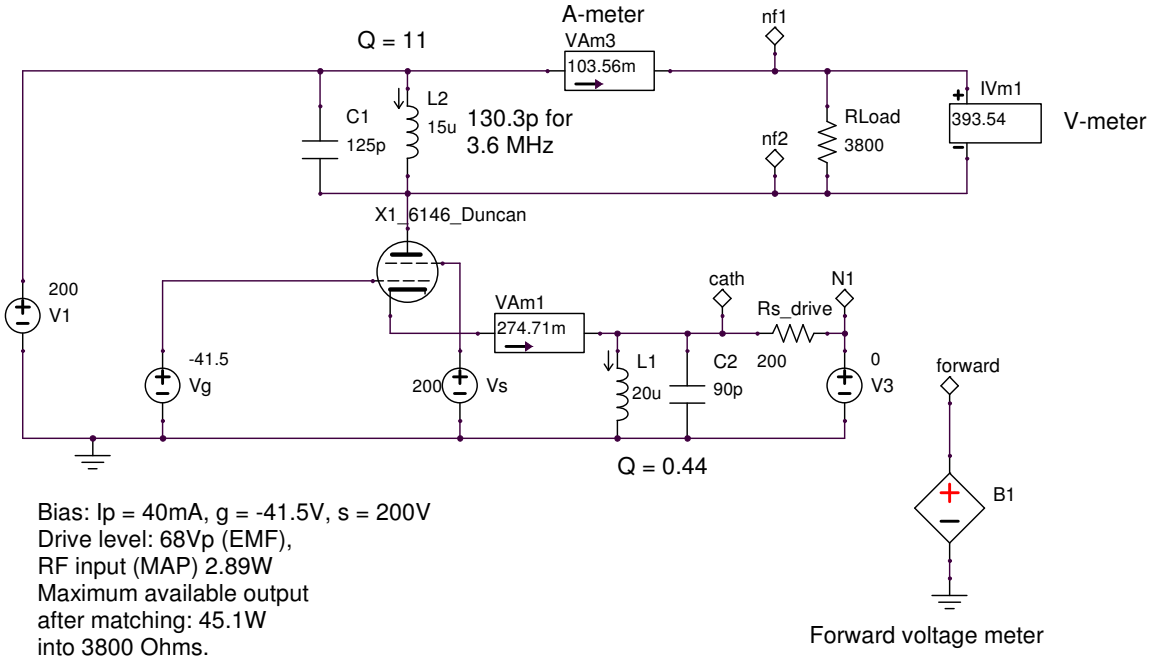
Simulation results for common grid single ended amplifier .

Below a circuit is given for a single ended Common Grid amplifier for 3.6 MHz. To enable others to do the simulation also, all unnecessary means are omitted. Also matching to 50 ohms is not present to avoid calculation of 50 Ohm load changes to plate load changes. Even screen current limiting is omitted.

The 1997 "Duncan" model for the 6146 valve is used (6146s.inc 13/8/97).

A forward voltage simulation is added also to examine forward voltage versus load change for non-50 Ohms load, just change the resistor value in the formula to change your wave impedance.

6146 class AB single-ended amplifier, 3.6 MHz.
6146amp3.ckt, Beige Bag Pspice A/D version 4.



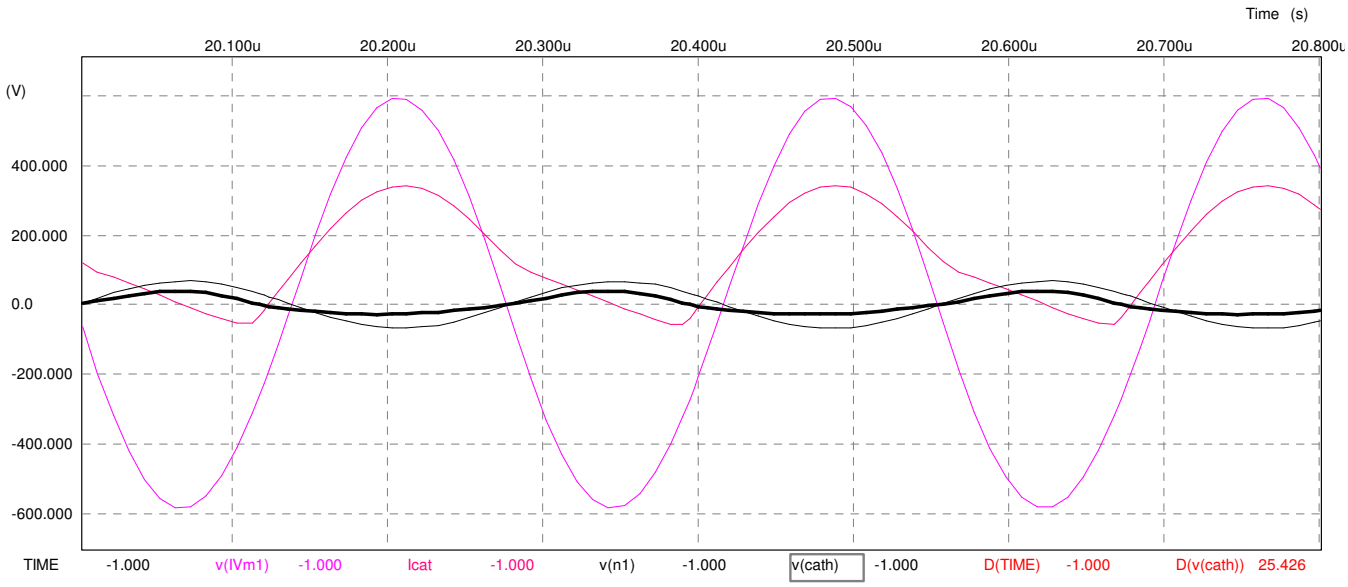
Bias: Ip = 40mA, g = -41.5V, s = 200V
Drive level: 68Vp (EMF),
RF input (MAP) 2.89W
Maximum available output
after matching: 45.1W
into 3800 Ohms.
Anode voltage: 586Vp

Gain = 15.6
Gain = 17.3 with 3dB drive reduction
Gain = 18.0 with 6dB drive reduction

Forward voltage meter

Forward voltage calculation for "forward" node
v = 0.5*(v(nf1) - v(nf2) + 3800*I(VAm3))

Next graph shows important voltages and currents for the amplifier.



purple = voltage across tank circuit (V(Rload))
red = cathode current (mA)
thick black = cathode voltage
thin black = EMF of source that serves as input (V3).

Conditions are as given in the circuit graph. Changing the capacitor or load resistor results in a drop of output power, so we have maximum output given a certain input condition. Why common grid? It is easy to match due to the low feedback from output to input and I built such at thing long ago with PL519 television tubes.

Behavior under maximum available power given certain drive.

Following results are for changing load resistance. This enables you to calculate the large signal output impedance of the amplifier. Actual calculation of impedance is done via ΔV/ΔI for small changes in load resistance. This gives good results for real output impedances. When the output impedance isn't real, this scalar method fails.

Load (Ohm)	3300	3600	3800	4000	4300
Load voltage (V)	533	568	586	596	604
Load current (mA)	161.5	157.8	154.2	149	140.4
Output power (W)	43	44.8	45.2	44.4	42.4
Output resistance (Ohm)	**9365**	**5046**	**1919**	**937**	

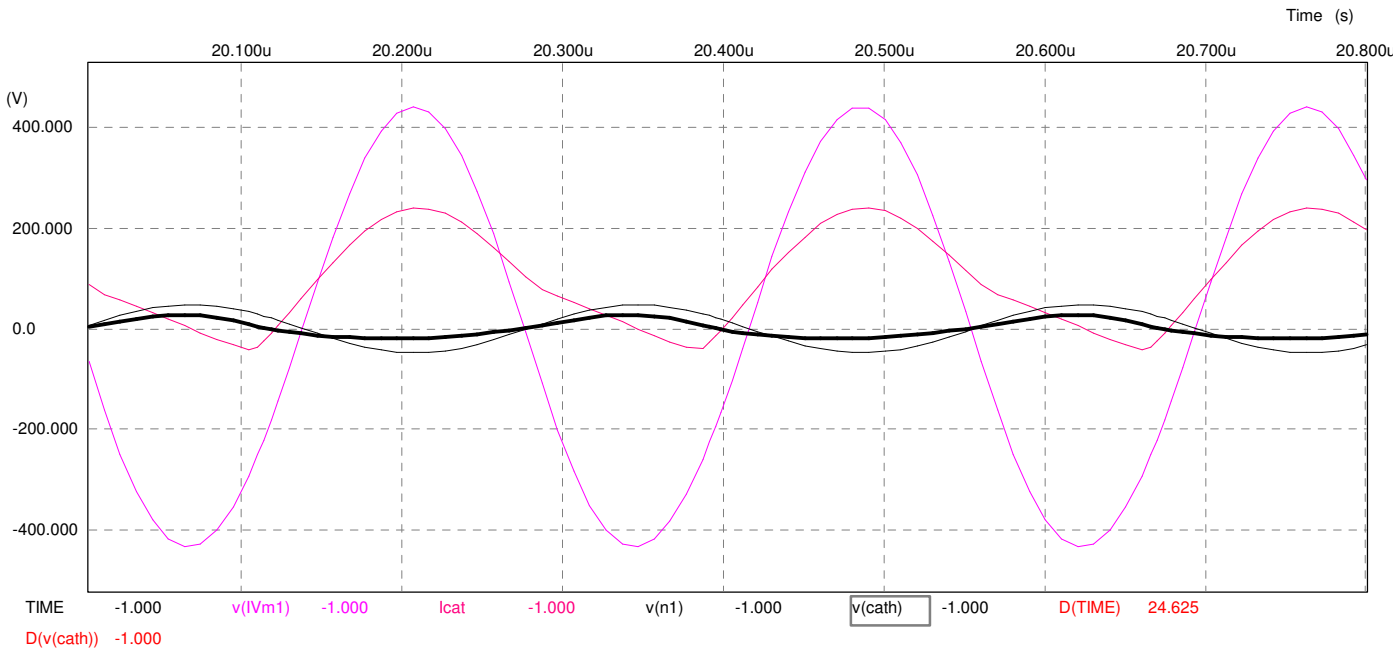
Load voltage based on half of p-p value, Current is calculated from load voltage.
Output resistance based on the current voltage/change between adjacent load resistances. So first value is based on first and second column values.

What can be concluded?
Result for this tetrode CG amplifier: small changes in load, give large change in output resistance. For the small load resistance, this is caused by current saturation (current is controlled by valve). For high load resistance, this is caused by voltage saturation effects (voltage dictated by supply voltage). The relative time where voltage saturation dictates, depends on the output voltage swing. Average between 5046 and 1919 is about 3500 Ohms, and close to the load impedance (output VSWR < 1.1).

This proves that under maximum output match and certain drive, there is a conjugated match, but under changing load (without retuning) large deviation does occur.

Reduced excitation.
Under SSB (or AM without supply voltage modulation), the average power delivered by the amplifier is far below the power level that is obtained after best match. So the amplifier is mostly used outside available power matched condition. Increasing the drive would result in strong envelope distortion with unacceptable splatter in case SSB or AM.

Following result is for 3 dB reduction in input drive (so we go from 2.89W to 1.44W maximum available source power).



purple = voltage across tank circuit (V(Rload))
red = cathode current (mA)
thick black = cathode voltage
thin black = EMF of source that serves as input (V3).

Results for varying load are given in the table below (EMF V3 = 48V):

Load (Ohm)		3600	3800	4000	
Load voltage (V)		416.6	437.6	457.9	
Load current (mA)		115.7	115.2	114.5	
Output power (W)		24.1	25.2	26.2	
Output resistance (Ohm)			**34k**		

Load voltage based on half of p-p value, Load current is calculated from load voltage.
The amplifier's output impedance is based on the upper and lower value for Rload.

When you do this simulation yourself, make sure your RELTOL setting is better then 0.2e-4, as you are looking to small difference between large figures. You may have to set maximum step size also to a lower value (for example 0.02us).

What can be concluded?
For this tetrode common grid amplifier under reduced excitation, output impedance is far from load impedance (output VSWR = 8.9). This is not strange for a tetrode amplifier. The addition of the screen makes the device acting more like a current source (as the screen reduces plate to gate interaction). Values of rd > 10k are not uncommon.

As the output voltage swing reduces to 70%, there is no voltage saturation influence anymore. So you are looking into the plate of a non-saturating valve over the full output voltage swing. The behavior is now fully dictated by the valve properties and parasitic or intended feedback.

Why is it so high in this circuit (around 30 kOhms)?
Now there is an impedance in the cathode, this provides series feedback reducing Re(Yplate) to above the valve's intrinsic value. In other words, Rplate (in a parallel equivalent circuit) increases.

Common Cathode single-ended amplifier example.

This one requires very much iterative steps (both R and Ctune, because of feedback to the grid where the input signal is applied). This causes the plate impedance to become more capacitive. This additional capacitance is not a real (non-dissipative) capacitance, but an electronically generated capacitance that exists of real dissipating electron current.

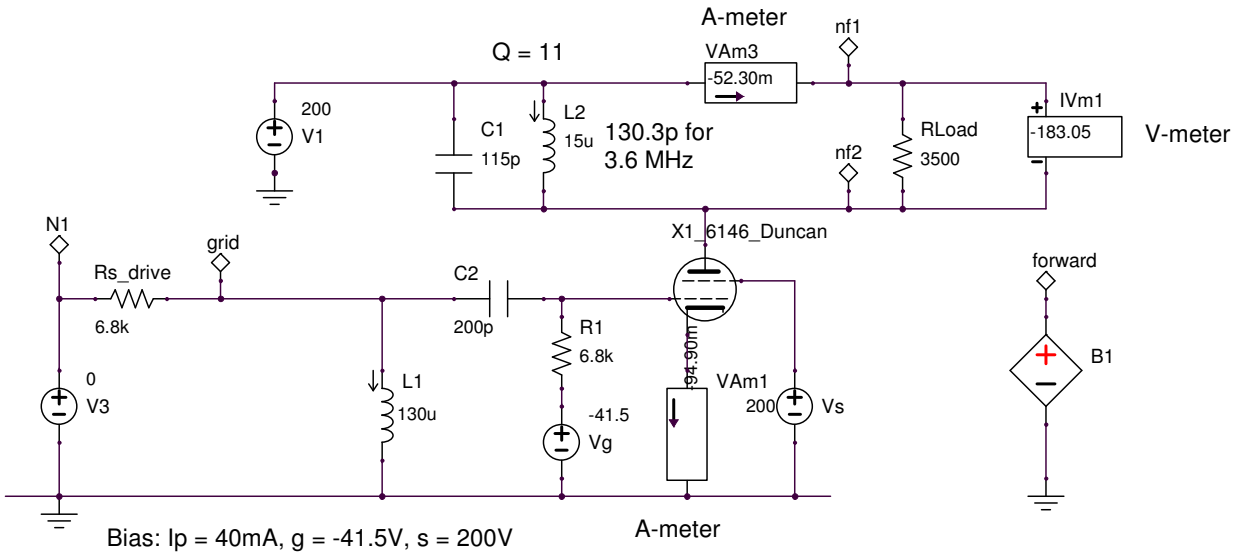
The amount (and phase) of feedback depends heavily on the source's impedance that drives the valve. Neutrodynisation could be used to make sure the maximum power matching would coincide with better phase between plate current and plate voltage.

Circuit is given below (together with the important waveforms).

Maximum output (with the given drive) appears at a large inductive load shown to the valve. This can be seen from the phase shift between current and voltage (voltage is in advance, so plate sees inductive load) and the capacitor (115 pF) is below the resonance value for the inductor. Increasing the capacitor to get better phase, results in reduction of output power.

6146 class AB single-ended amplifier, 3.6 MHz.

6146ampCC1.ckt, Beige Bag Pspice A/D version 4.



Bias: Ip = 40mA, g = -41.5V, s = 200V
Drive level: 70Vp (EMF),

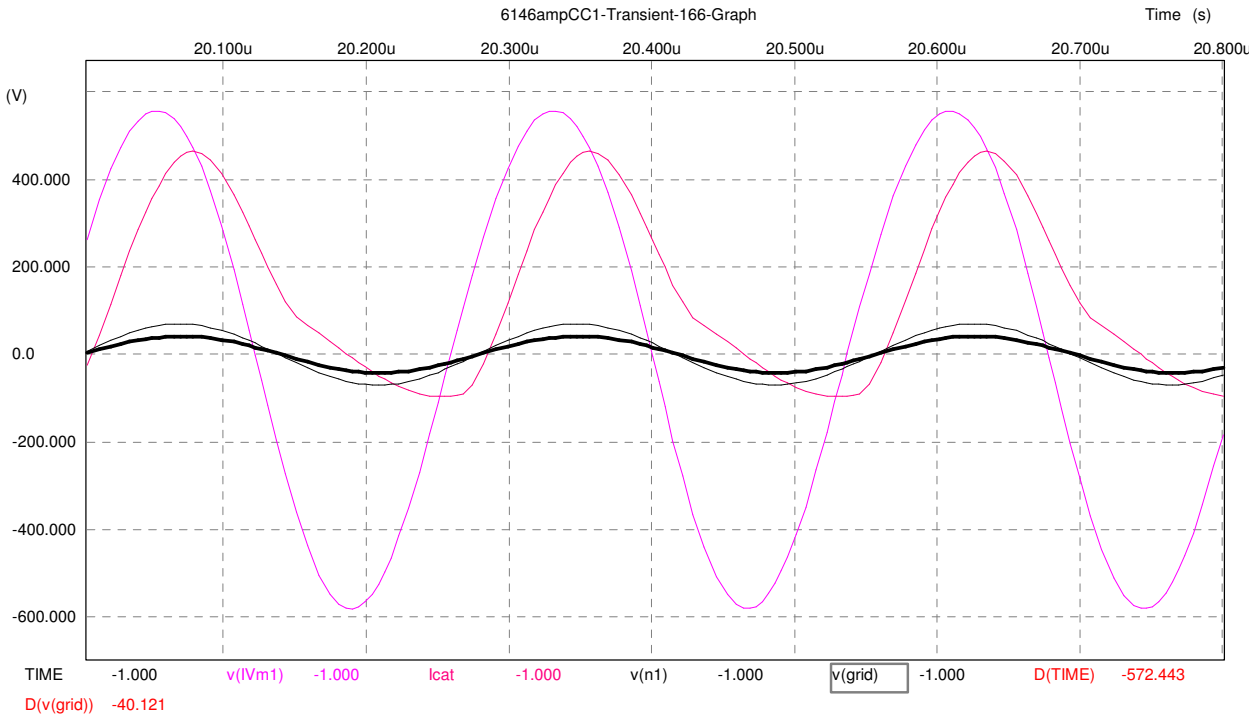
after matching: 46.3W
into 3500 Ohms.
Anode voltage: 569Vp

output = 23.5W at -3dB reduced drive.

Forward voltage meter

Forward voltage calculation for "forward" node
v = 0.5*(v(nf1) - v(nf2) + 3500*I(VAm3))

Relevant waveforms (from simulation):



purple = voltage across tank circuit (V(Rload))
red = cathode current
thick black = grid voltage
thin black = EMF of source that serves as input (V3).

Simulation results under varying load

Results for varying load are given in the table below (EMF V3 = 70V):

Load (Ohm)	3200	3500	3800
Load voltage (V)	513.5	569.0	583.5
Load current (mA)	160.5	162.6	153.6
Output power (W)	41.2	46.3	44.8
Output resistance (Ohm)	**26.4k**	**1.6k**	

Load voltage based on half of p-p value, current calculated from load voltage.
Output resistance based on difference between column value en right next column value. So first value is based on first and second column.

Optimum impedance is probably around 3600 Ohms, looking to the decrease in power.

What can be concluded?
Output impedance varies significantly with small change in load (load change less then VSWR=1.1). The high output impedance is because of current saturation of the tetrode and the low output impedance due to voltage saturation.

Plate voltage is significantly out of phase reducing efficiency.

Reduced excitation.
Excitation (maximum available power from driving source) is reduced with 3 dB.

There seems a very small reactive component present in Zout, as a small change in tuning capacitor gives small increase of output power (this may also be caused by a gain change). The capacitor has not changed, so is still 115pF.

To have reliable results with load pulling with scalar measurements, one has to make sure that the output impedance is real. Any parallel inductance or capacitance would result in a reduction in |Zout|, masking the real part (in a parallel equivalent circuit).

Load (Ohm)		3200	3500	3800	
Load voltage (V)		373.7	405.9	436.9	
Load current (mA)		116.8	116.0	115.0	
Output power (W)		21.8	23.5	25.1	
Output resistance (Ohm)			**35k**		

To be honest, I did not expect this high value as there is no cathode impedance anymore.

What can be concluded?
Also for the CC case, the output impedance in the current saturation mode (reduced input drive) deviates significantly from the load impedance (VSWR = 10).

Reactive output impedance.

Simple load change scalar measurements fail under reactive load. You can try this yourself by applying the load change method on a voltage source in series with a capacitor with 50 Ohms reactance. You will not be able to figure out that the impedance is fully reactive (so output VSWR = infinite).

To find out what Zout is (or output VSWR), you need to "show" the amplifier various (complex loads). Also in simulation this takes long if you have to run various simulations to find the required data to do the calculation. To get some good estimate, you require over 10 different loads.

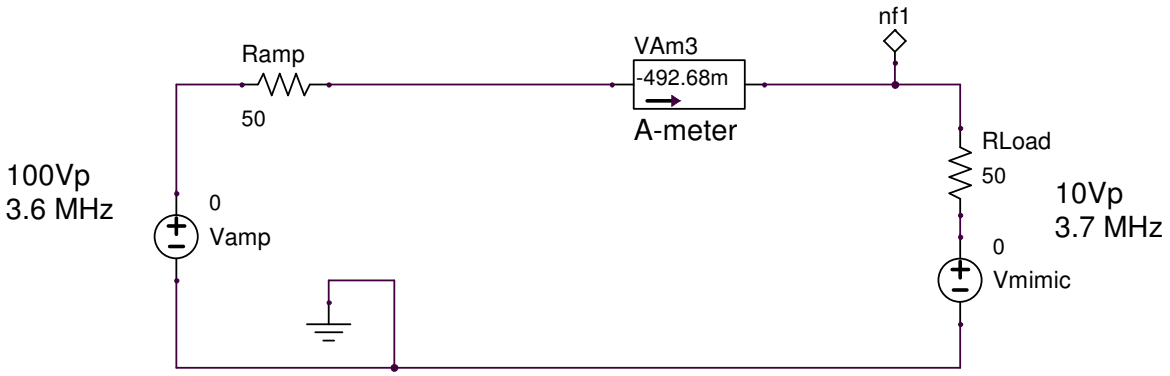
One can change the angle of VSWR (or angle of reflection coefficient) in a single simulation by adding a source that mimics the reflection from the load resistor towards the amplifier. By having a small frequency difference between the amplifier's input and the "mimic" source, the "mimic" source will pass all phase angles. We have a time varying reflection coefficient now! If the frequency of the injected signal equals the drive signal frequency, you have a steady state mismatch (this is called "active load pulling").

One can also say, you send a wave towards the amplifier with different frequency, so you can separate the wave generated by the amplifier itself and the reflected wave (with somewhat different frequency). Now you have a standard VNA setup.

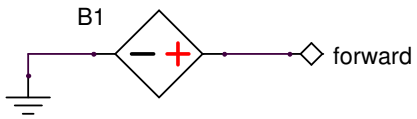
Basic circuit is given below:

Measurement of output VSWR

VSWRout_meas1.ckt, Beige Bag Pspice A/D version 4.



Forward voltage meter for Vamp



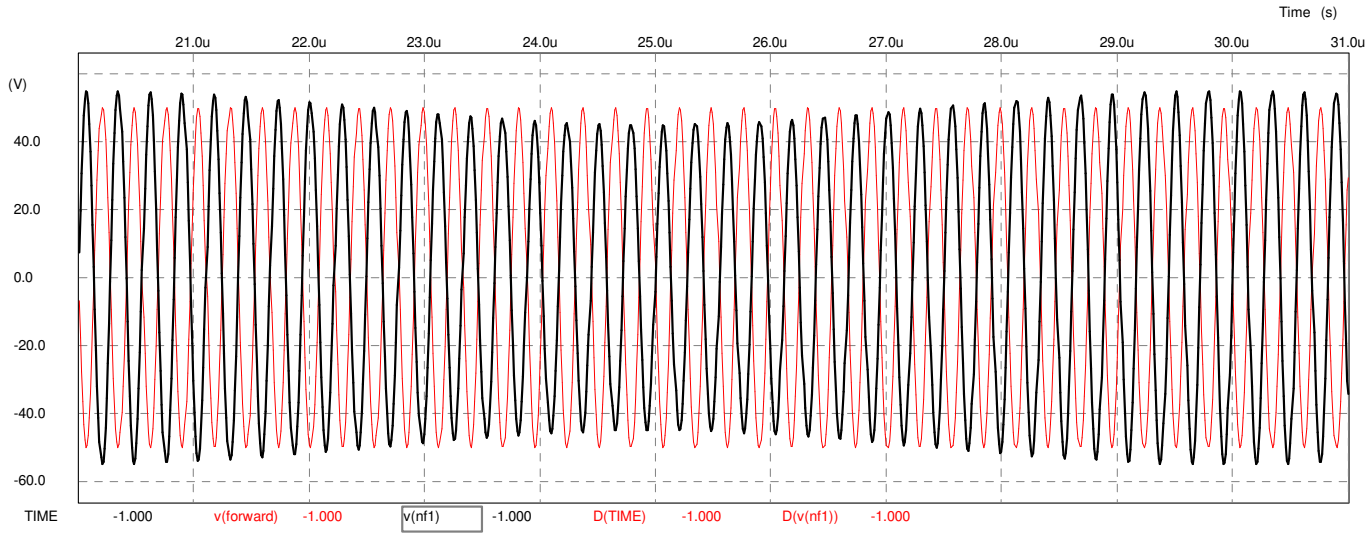
Forward voltage calculation for "forward" node
v = -0.5*(v(nf1) + 50*I(VAm3))

Vamp provides a forward wave (to right) of 50Vp, 3.6 MHz into 50 Ohms (25W). Vmimic provides a forward wave (to left) of 5Vp, 3.7 MHz into the output impedance of the amplifier (Ramp).

The "forward" voltage indicator, indicates the voltage wave that travels to right direction only, so it doesn't see things going to left direction.

After: 1/(3.7MHz-3.6MHz) = 10us, the phase of Vmimic travels 360 degrees with respect to the phase of Vamp. So the reflection coefficient seen by the amplifier travels 360 degrees at the smith chart. "Effective" |RC| = 5/50 = 0.1 (VSWR = 1.11)

The effect of this on the forward voltage (traveling to right) and V(nf1) has been simulated (result given below).



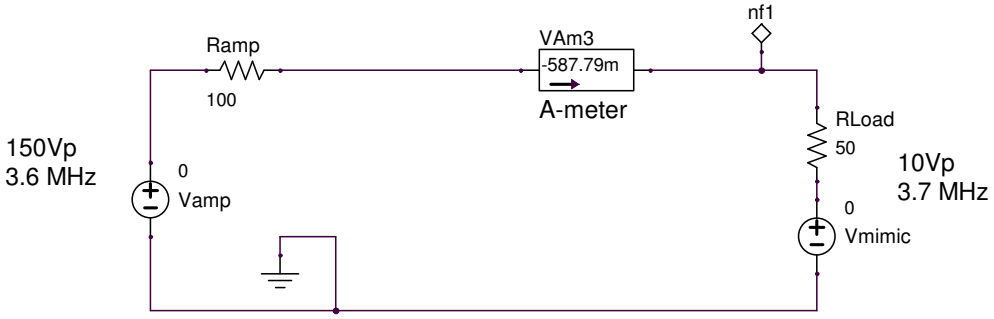
red = minus forward voltage (to make it better visible), 50Vp
black = voltage at node nf1, amplitude varies between 44.8 and 54.9V

As there is no reflection from the amplifier towards Rload, "forward" will only show the output of the amplifier, hence 50 Vp. Due to the small frequency difference, voltage wave of Vmimic interferes with voltage wave of Vamp with continuously varying phase. Therefore you get maximum destructive and maximum constructive interference each 10us interval.

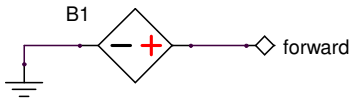
Now we change to Vamp = 150V, Ramp = 100 Ohms. Power supplied to 50 Ohms is still 25W. The forward wave of Vmimic (goes to left) will cause reflection (goes to right) that will be detected by the forward voltage indicator "forward".

Measurement of output VSWR

VSWRout_meas2.ckt, Beige Bag Pspice A/D version 4.

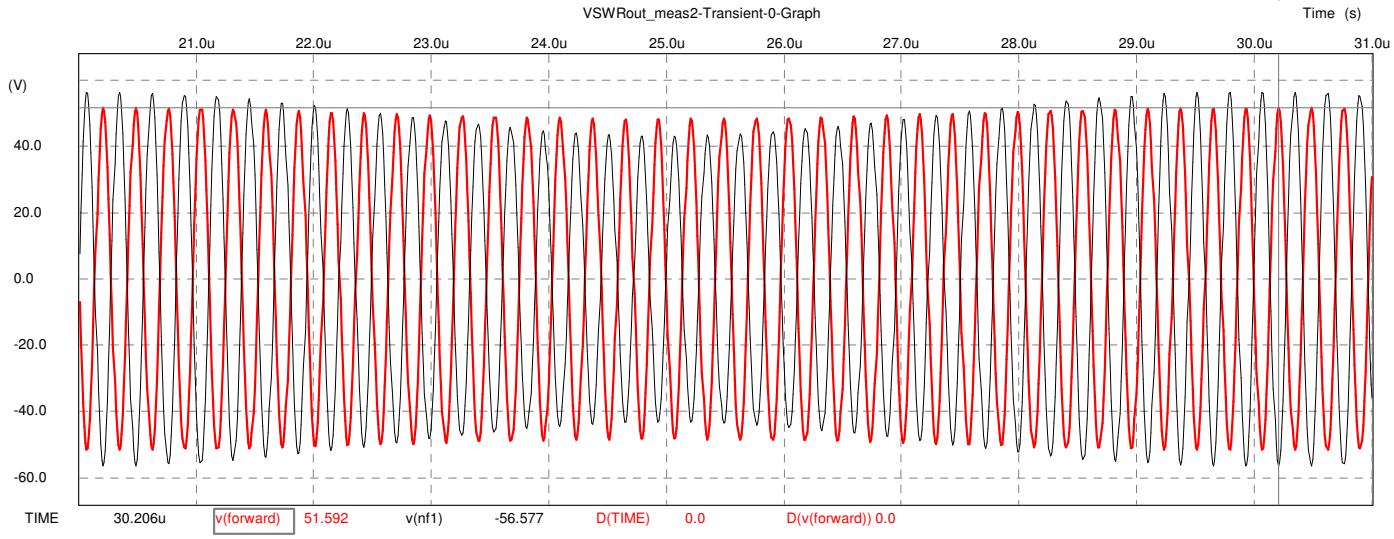


Forward voltage meter for Vamp



Forward voltage calculation for "forward" node
v = -0.5*(v(nf1) + 50*I(VAm3))

Simulation results:



red = forward voltage, amplitude is between 48.1 and 51.5V.
Black = voltage at node nf1, amplitude is between 43.1V and 56.5.

Now both V(nf1) and "forward" voltage do change due to the interference between different frequency voltage waves.

Analysis:

Vmimic forward voltage (into 50 Ohms) = Vf.mimic = 5V.

Reverse Vmimic voltage = Vr.mimic = (max.amplitude – min.amplitude)/2

Vr.mimic = (51.5-48.1)/2 = 1.7V

|RC| = Vr.mimic/Vf.mimic = 1.7/5 = 0.34

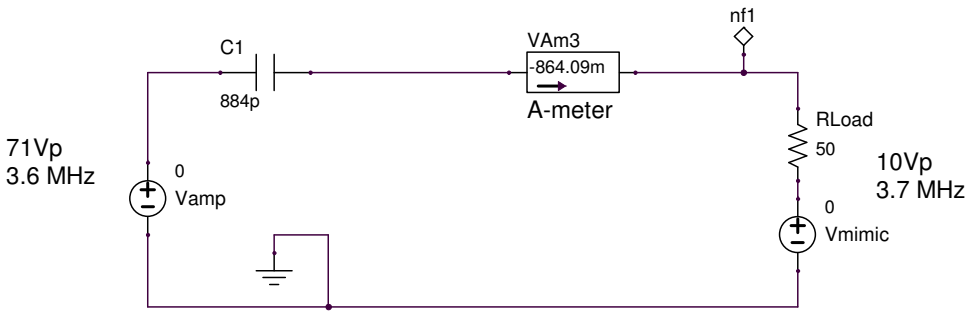
Output VSWR = (1+0.34)/1-0.34) = 2.03.

A 100 Ohms source has a VSWR = 2 (referenced to 50 Ohms), so this is not a bad result.

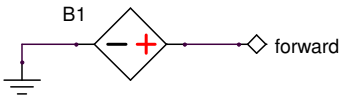
Now we change to a fully imaginary source with EMF = 71V and -j50 Ohms (884pF) in series (delivers 25W into 50 Ohms).

Measurement of output VSWR

VSWRout_meas3.ckt, Beige Bag Pspice A/D version 4.

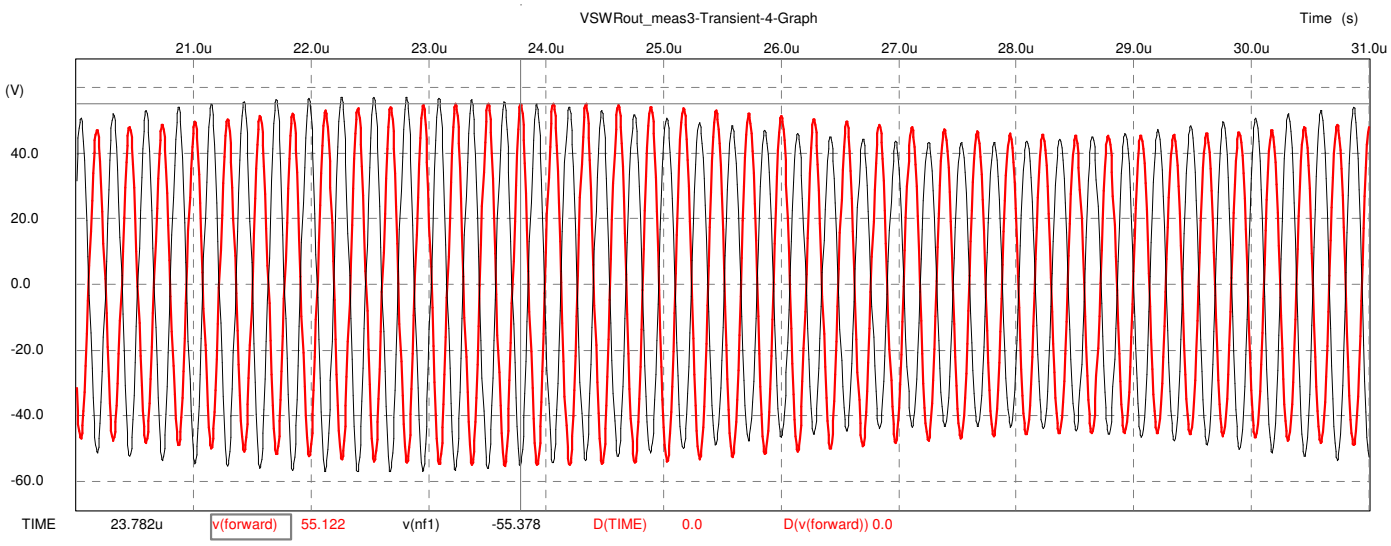


Forward voltage meter for Vamp



Forward voltage calculation for "forward" node
v = -0.5*(v(nf1) + 50*I(VAm3))

Simulated waveforms are shown on next page



Red = forward voltage, amplitude is between 45.2V and 55.2V
Black = voltage at node nf1, amplitude is between 43.4V and 57.2V

Analysis:

Vr.mimic = (55.2-45.2)/2 = 5V.

|RC| = Vr.mimic/Vf.mimic = 5/5 = 1

VSWR = (1+1)/(1-1) = infinite

This is as expected, a capacitor is on the edge of the Smith Chart.

All values mentioned under the graphs have been obtained after zooming onto the maximum/minimum amplitudes.

This method was also applied to the common cathode valve amplifier. Results agree with the results obtained with the load change method (VSWR>10).

Hints.

Now we have a simple method to simulate the output VSWR of a circuit, by using a relative small signal that is driven into the amplifier. There are some things you should consider to avoid unreliable results:

1. For finding maximum and minimum values with a marker, you may increase the zoom factor to avoid dot-joining issues because of limited amount of display pixels with respect to the length of the data record.
2. Play with accuracy (RELTOL, Step Ceiling) to see whether there are changes. When you use a small ratio of (Vf.mimic/Vfamp), you have a small difference between large quantities, sensitive to significant errors.
3. Mostly about 20 swings between two maxima or two minima are sufficient. That means the difference between the two frequencies can be around $\Delta f = 0.05 \cdot fcenter$. The time between two maxima equals $t = 20/fcenter$.
4. The frequency of Vmimic must be well within the pass band of the amplifier. When simulating a circuit with a high loaded-Q, you need to reduce the relative frequency difference. This results in more swings between minima/maxima, hence longer simulation runs.
5. When having a small number of swings between maxima, the most accurate maximum and minimum maybe in the negative amplitudes. Don't mix readings from both negative and positive amplitudes, so use all positive or all negative values for determining the amplitudes (this is because of distortion in the amplifier's output).
6. This method works for all circuits with either complex or real output impedance.
7. You can use Vf.mimic = 0.05·Vf.amplifier as start, this presents a VSWR = 1.11 to the amplifier. Note that EMF is twice the forward voltage value, so if you want Vf.mimic = 20V, Vmimic must be 40V.
8. If the envelope of the output from the forward coupler isn't sinusoidal, the output impedance is very sensitive to load change. In that case you should reduce Vmimic. This may result in accuracy issues (increase RELTOL and/or maximum step size).
9. Make sure that there is no DC variation in the output of the amplifier. A sign of DC is when the negative envelope isn't in opposite phase with the positive envelope. If problems, add a BPF. This is also good to reduce harmonics.
10. First simulate with Vmimic = zero. This is to observe that during the observation interval the output of the amplifier is stable. Therefore it is also advised to have at least 2 maxima or minima in your result window to check for validity of the results.
11. If you are working with non-50 Ohms systems, make sure that you don't forget to change the constant in the "forward" voltage formula. This coupler has no output attenuation. If you use a standard coupler from a library, you have to multiply all amplitudes with the coupler's attenuation (not in dB's). It is advised to run a test simulation with known output impedance to verify your setup.

Real Load Change / Pull measurement/simulation.

If you have more confidence in changing loads (load pulling), it can be done, but you have to determine the phase change (for example with respect to the driving source, or comparing with the previous simulation). Zero crossings are best to determine the time delay accurately. A calculation example is given below:.

Load change/pull simulations/measurements

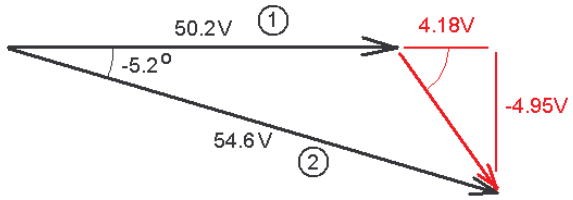
"Unknown" output impedance of certain network simulation results:

Situation 1: 50.2Vp into 50 Ohms, so current = 1.004Ap

Situation 2: 54.6Vp into 60 Ohms with 4ns delay w.r.t. situation 1, so current = 0,910Ap

All at 3.600 MHz

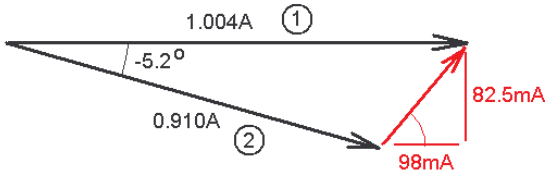
Phase difference between 2 and 1 = 3.6MHz * -4ns *360 = -5.2 degrees.



cos comp: 54.6*cos(-5.2) - 50.2 = 4.18V
sin comp: 54.6*sin(-5.2) = -4.95V

|ΔV| = 6.48V
Arg(ΔV) = -49.8°

|ΔV| = sqrt(4.18^2 + 4.95^2) = 6.48V
Arg(ΔV) = invtan(-4.95 / 4.18) = -49.8°



|ΔI| = 0.128A
Arg(ΔI) = +40.1°

|Zout| = 6.48V / 0.128A = 50.6 Ohm
Arg(Zout) = -49.8 - 40.1 = -89.9°

Re(Zout) = 50.6*cos(-89.9) = 0.1 Ohm
Im(Zout) = 50.6*sin(-89.9) = -j50 Ohm (870pF)

Actual circuit was a voltage source 3.6 MHz, 71Vp with 884 pF capacitor in series.
In case of ignoring the phase difference, one would find |Zout| = 47 Ohms without any phase info.
It is clear that you need to include phase.

A spreadsheet doing the math is available on request at *wimtel@tetech.nl.*

This method is very sensitive to phase errors, as under load changes of about VSWR = 1.2, phase change is just some degrees, even for strong reactive output impedances.

7 MHz, 100W common source mosfet amplifier simulation.

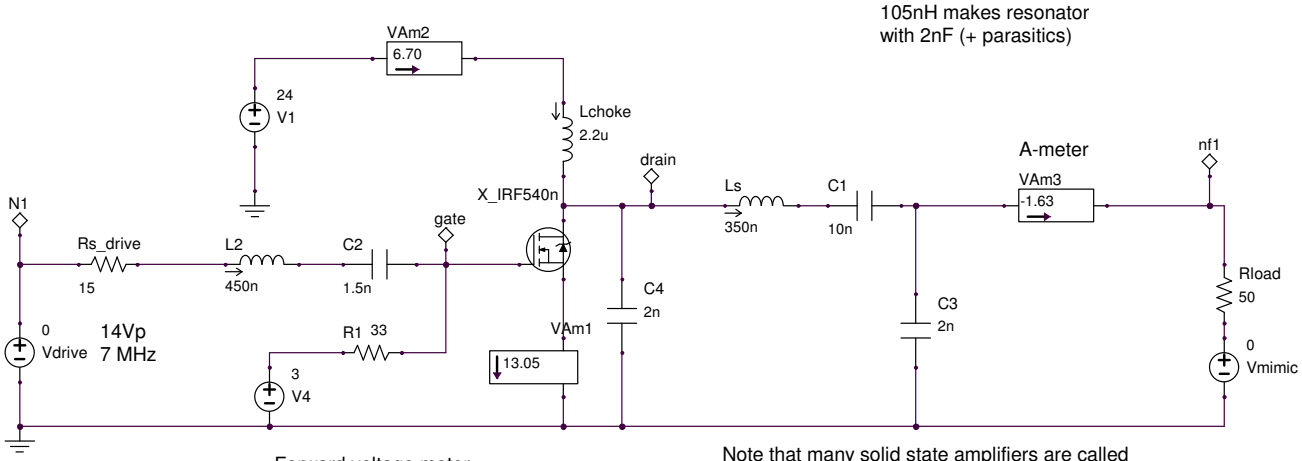
This circuit is strongly saturated Class C amplifier with IRF540N mosfet operating at 7 MHz (**¡intended for simulation only!**). Input matching to 50 Ohm has not been carried out, but matching to 50 Ohms is present (L-match). The circuit is given below with relevant waveforms. The waveforms look like it is a class E stage.
02-July-2010, input drive circuit changed to avoid envelope instability under certain load conditions.

IRF540N class C amplifier, 7 MHz
IRF540N_classCamp1.ckt, Beige Bag Pspice A/D version 4.

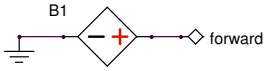
¡Circuit is for simulation purpose only!

Qloaded = 4.4 and transforms 2.46 Ohms to 50 Ohms
lmatch = 245nH

105nH makes resonator with 2nF (+ parasitics)



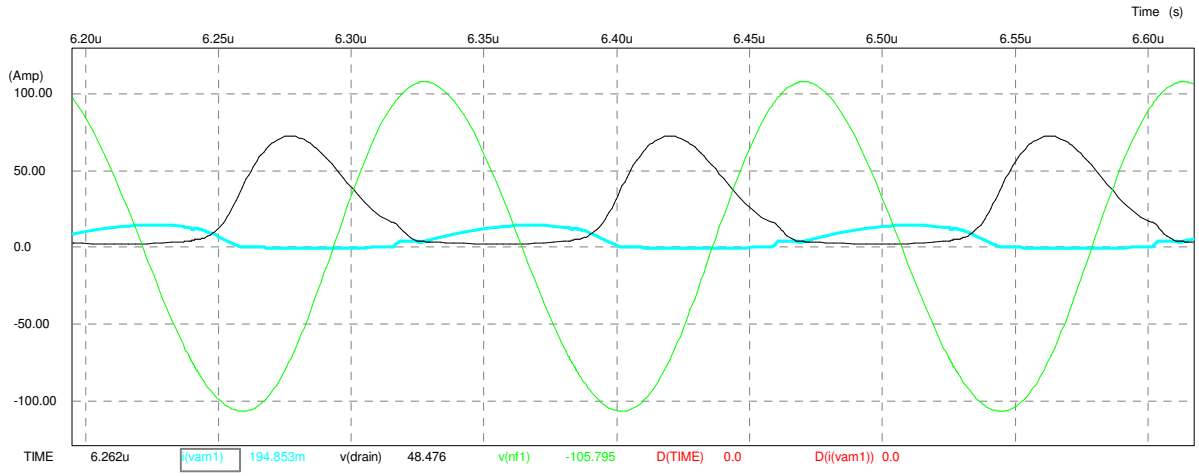
Forward voltage meter



Forward voltage calculation for "forward" node
v = -0.5*(v(nf1) + 50*I(VAm3))

Note that many solid state amplifiers are called "class C", but because of the low impedance levels it is hardly possible to get real class C operation, many of these amplifiers are (semi) saturating.

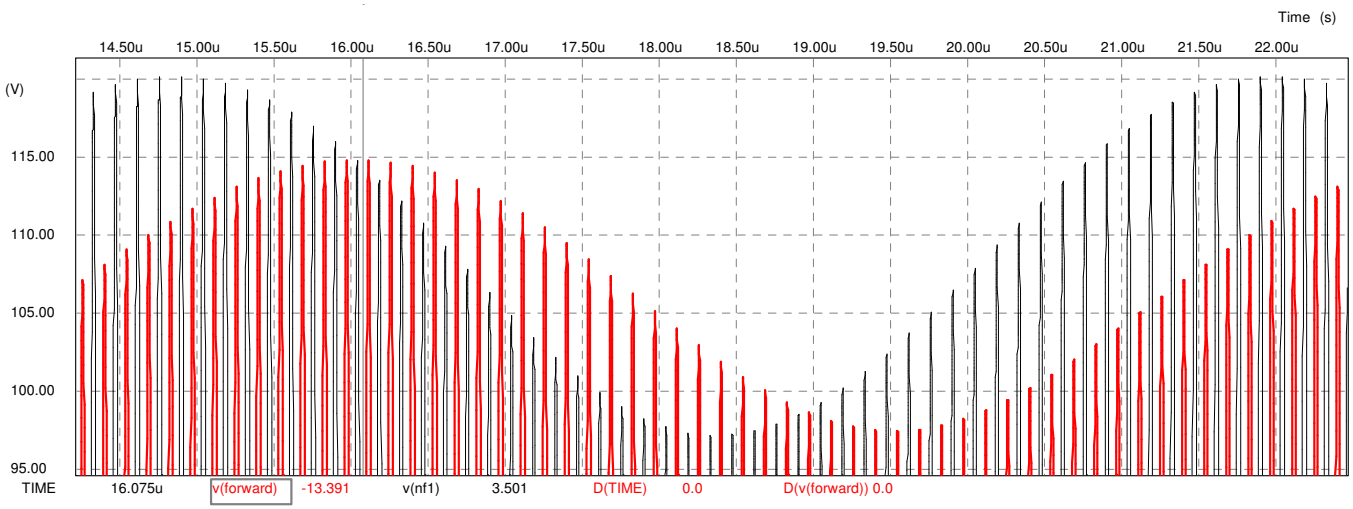
This design is also saturating.
Some data: output power at 14V drive (Pin.av = 0.9W)
Pout = 114W, DC input: 24V, 5.77A.
Drain efficiency: >80%.



Blue = source current, Black = drain voltage, Green = output voltage (nf1) ,Vmimic = 0.

Output impedance.
Output voltage into 50 Ohms is about 110V, we start with 10Vp voltage, 7.14 MHz that is sent into the amplifier (so Vmimic = 20Vp). This presents VSWR=1.2 with varying phase to the amplifier. To make the forward voltage better visible, the output is inverted (minus sine). Note that there is a series resonant circuit between C3 and the A-meter (227pF, 2.27uH, Q = 2) to block "slow" varying DC.

As the loaded Q of the matching is 4.4, 7.14 MHz is within the operating frequency range of this amplifier. Waveforms with Vmimic present are shown below:



red = forward voltage, amplitude varies between 97.4V and 114.8V
black = voltage at nf1 varies between 97.2V and 120.2V, envelope is 1.187us in advance (w.r.t. red trace).

There is no strong distortion in the envelope of the forward voltage, so Vf.mimic = 10V is an acceptable value. Actual values are obtained after zoom function in display module of B^2 Spice.

Output VSWR calculation:

Vr.mimic = (114.8-97.4)/2 = 8.7Vp, Vf.mimic = 10Vp.

|RC| = 8.7/10 = 0.87

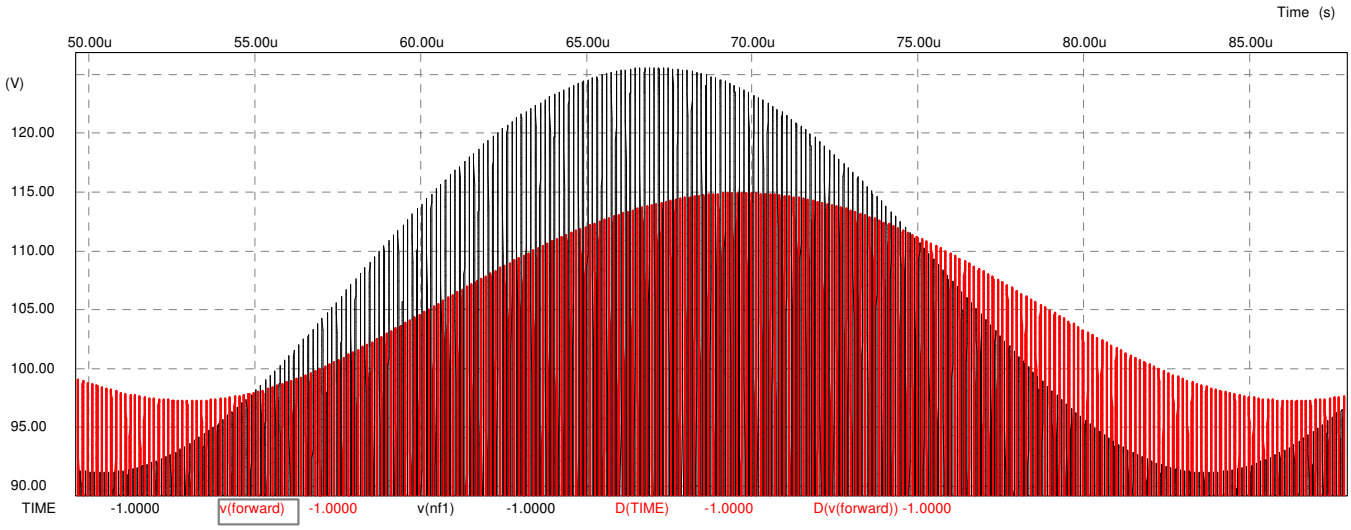
Output VSWR = (1+0.87)/(1-0.87) = 14

This equals an output resistance of 3.6 or 700 Ohms when the cable length between amplifier and load is such that you are on the real axis of the Smith Chart.

From the delay between the Vr.mimic envelope and envelope of (Vr.mimic + Vf.mimic), actual output impedance can be calculated:

Zout = 6.8 – j37 Ohms (|RC|=0.84 Arg(RC)=-106^0)

Now same measuring method, but with 30 kHz difference frequency:



red = forward voltage, amplitude varies between 97.3V and 114.8V
black = voltage at nf1 varies between 91.2V and 125.6V, envelope is 2.578us in advance (w.r.t. red trace).

Output VSWR calculation:

Vr.mimic = (114.8-97.3)/2 = 8.75Vp, Vf.mimic = 10Vp.

|RC| = 8.7/10 = 0.875

Output VSWR = (1+0.875)/(1-0.875) = 15

From the delay between the Vr.mimic envelope and envelope of (Vr.mimic + Vf.mimic), actual output impedance can be calculated:

Zout = 21.3 – j101 Ohms (|RC|=0.85, Arg(RC)=-51^0)

Now Vmimic is reduced from 20 to 10V, frequency difference remains 30 kHz. So the reflection coefficient seen by the amplifier is:

$|RC|_{\text{seen by amplifier}}$ = 5/110 = 0.0455 (VSWR = 1.10).

Red trace envelope = 8.8Vpp, Black trace envelope = 17.1Vpp, red trace is 2.568us behind:

Zout = 18.8 – j101 Ohms (|RC|=0.86, Arg(RC)=-51^0)

The output impedance seems linear as relative large change in VSWR, doesn't change output impedance much (for the difference frequency method). Is this actually true or not?

A load pull/change measurement will be done. Changing from 40 to 60 Ohms load (accounting for phase shift in output voltage) shows

Zout = 123 + -j199 Ohms (|RC|=0.81, Arg(RC)=-20.8^0).

Now we add a 1/8λ, 50 Ohms line between the output of the amplifier and the load pull measurement. This will change the phase of the reflection (as seen by the amplifier) with -90^0. It will also add -90^0 in the measurement result for reflection coefficient, so this must be corrected. Simulation shows:

$Zout_{(1/8\lambda)}$ = 9.6 + -j21.6 Ohms (|RC|=0.73, Arg(RC)=-132^0).

Rotating this impedance over +90 degrees on the smith chart gives:

Zout = 53 + -j108 Ohms (|RC|=0.73, Arg(RC)=-42^0).

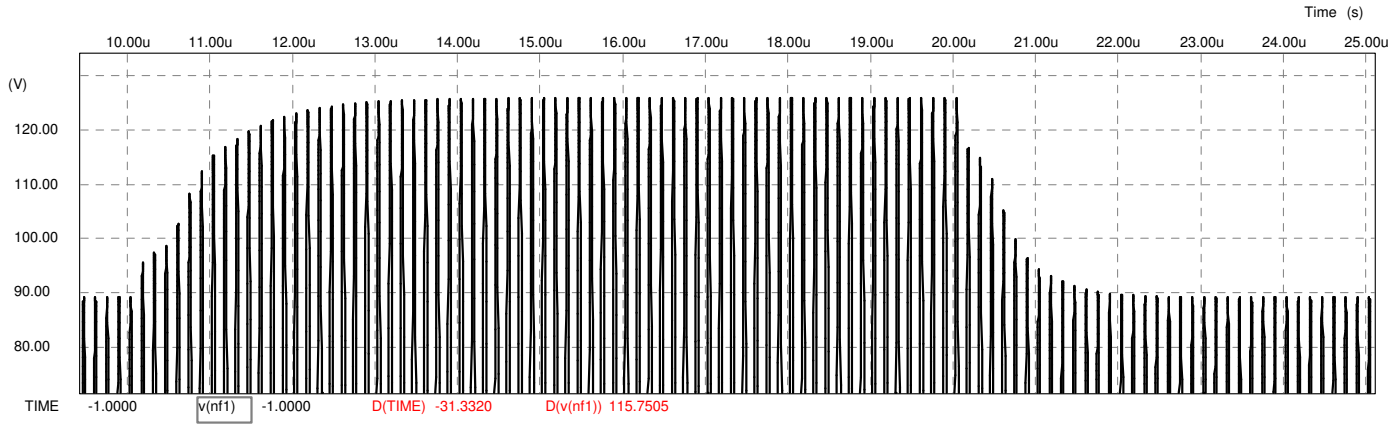
Changing the phase of the load pull changes the output impedance. As soon as an active devices goes into saturation, or will be close to saturation where capacitances become strongly voltage dependent, the system becomes strongly non-linear and the output impedance depends heavily on how it is measured.

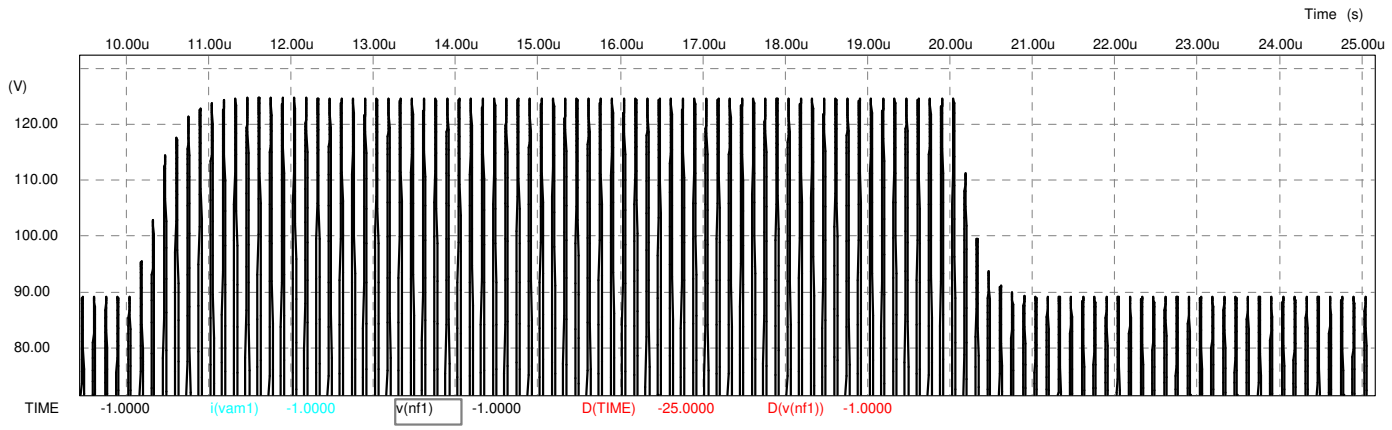
There is another aspect that can be of interest.

Zout = 6.8 – j37 Ohms (|RC|=0.84 Arg(RC)=-106^0) measured with 140 kHz offset and phase changing VSWR=1.2.
Zout = 21.3 – j101 Ohms (|RC|=0.85, Arg(RC)=-51^0) measured with 30 kHz offset and phase changing VSWR=1.2.

Why there is large difference in these results, as both frequencies are far within the pass band of the amplifier? The reason is the 2.2uH choke in the amplifier; it impedes rapid supply current changes.

Below the output voltage (V(nf1)) is shown for a load step from 40 to 60 Ohms and vise versa (directly presented to C4, so no coaxial line and LC series circuit present). As the Q factor of the matching network is about 4.4, the expected -3 dB bandwidth of the matching network would be about 7M/4.4 =1.59 MHz. This would result in 36% decay of about 200ns. The graph shows a decay of about 700..800ns.





The output voltage response to the same load step (40 to 60 Ohms and vice versa) is shown above, but with Lchoke = 0.25uH parallel with 1.3nF. 1.3nF is necessary to restore the same drain waveform.

In this graph, steady state is reached more then twice as fast. So actual bandwidth for varying load (also for varying input signals) is not only determined by the filters, but also by (for example) chokes that impede fast current changes that are required for fast changing output power. This is an issue in multiple carrier amplifiers also.

The response of the first graph matches that of an amplifier with a -3 dB bandwidth of about 400 kHz (VSWR=2 bandwidth would be 280 kHz). In such a case using 7.14 MHz difference frequency while the center is at 7 MHz disables the amplifier to settle to the presented varying load VSWR. This is the mayor cause of difference in simulated Zout using the difference frequency method. Therefore a second simulation was carried out using 30 kHz.

Conclusion:
In this amplifier topology, that is not uncommon nowadays, the output VSWR >> 1. Also shown that actual results depend strongly on the measuring method used. Comparing measurements is only possible when the setup is described in detail. For static/passive load pulling, even cable length is of importance, as phase angle of reflection coefficient presented to the amplifier may change output impedance.

Class AB LD mosfet output stage, single ended, 145 MHz.

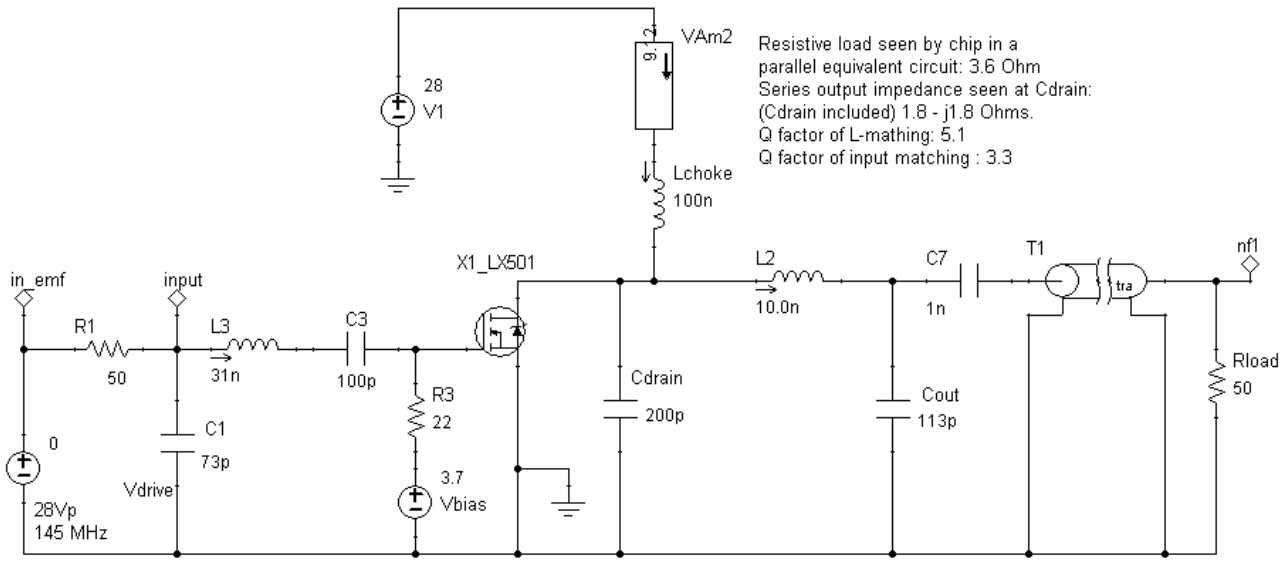
The circuit below is a 2m band linear amplifier capable of >100W saturated output. As it is used as linear amplifier, impedance simulation are carried out at non-saturated output power. Saturated output power at 4W input is about 168W (in simulation), but with high risk of exceeding DS breakdown voltage.

Tuning in simulation is based on on-chip drain to source voltage and charge carrier current through the JFET that is part of the Polyfet LX501 LD MOST spice model. This model also includes package parasitics and therefore actual drain voltage and current (as measured at the package terminals) does not represent real drain voltage and current. Cdrain and Cout follow from calculation, L2 is used for tuning to have internal Vds in phase with internal Id.

Both input and output is transformed to 50 Ohm system impedance.

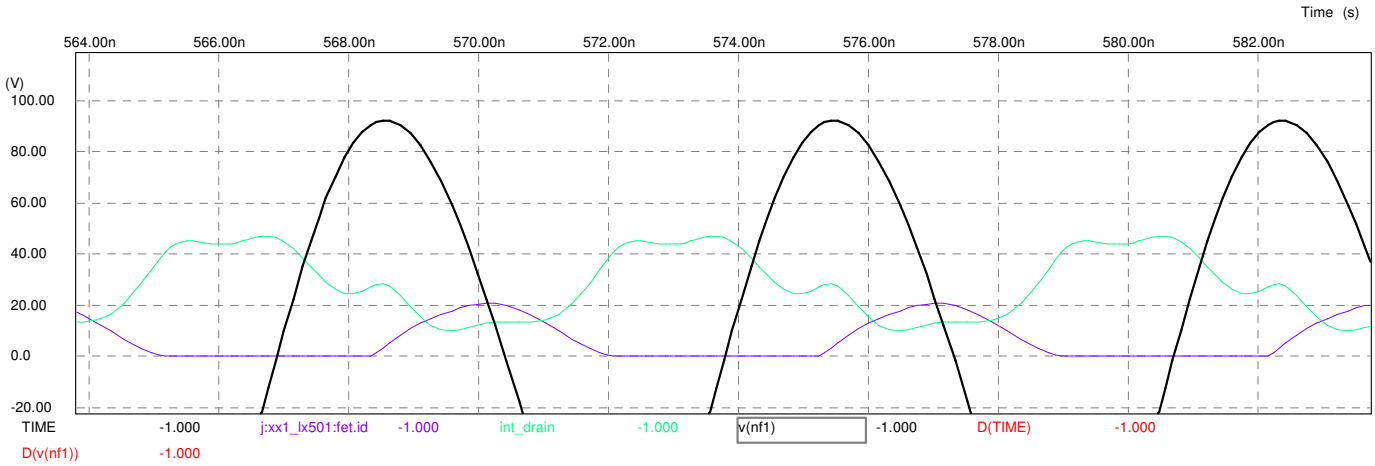
Single ended 145 MHz class AB amplifier > 80W

singleamp145MHz1.ckt, Device: PolyFet LX501



Transmission line length (T1) is not present unless otherwise noted.

Relevant waveforms are shown below:



black = output voltage (V(nf1)) (V)
Blue = charge carrier current through drain of LD MOST (A)
Green = on chip drain-source voltage (V)

Key data: with 50 Ohms load.

Output power (based on pp output voltage) = 89.7W
Available input power out of 50 Ohms: = 2.0W.

Input current (at 28Vdc) = 6.65A, Input power = 186W
Efficiency = 48%.

Though some third harmonic peaking is present, this was no design objective.
Increasing drive level does increase efficiency significantly.

Output impedance:
VSWR=1.2 load pulling is used, all 145.0 MHz, no transmission line present:

42.5 Ohms:

Vout = 92.0V, zero crossing: 501.491ns
No drain saturation present

Output power = 99.6W
DC Input current = 6.52A
Efficiency = 55%.

60 Ohms:

Vout = 97.4V, zero crossing: 501.405ns

Output power = 79.1W
DC Input current = 6.75A
Efficiency = 42%.

Zout = 5.8 + j15.3 Ohms (|RC| = 0.81 Arg(RC) = +146^0)

Load pulling VSWR=1.2, but with 1/8λ, 50 Ohm line in series, this changes the phase of VSWR shown to the amplifier with -90^0.

42.5 Ohms:
Vout = 84.1V, zero crossing: 502.374ns
No drain saturation present

Output power = 83.2W
DC Input current = 6.68A
Efficiency = 44%.

60 Ohms:
Vout = 107.3V, zero crossing: 502.230ns

Output power = 95.9W
DC Input current = 6.61A
Efficiency = 52%.

$Zout_{1/8\lambda}$ = 13.4 + j83.4 Ohms (|RC| = 0.87 Arg(RC) = $+61^0$)

After phase correction for the 1/8λ line, output impedance for VSWR=2, is:

Zout = 3.8 + j12.8 Ohms (|RC| = 0.87 Arg(RC) = $+151^0$)

Though the output impedance is far from 50 Ohms, it is not very sensitive to change in (small) load VSWR phase angle. It should be noted that in all cases the amplifier did not go into saturation (lowest drain voltage about 7V).

Conclusion.
Output impedance of this non-saturated amplifier is far from 50 Ohms (VSWR >> 1). Due to the drain voltage headroom, VSWR = 1.2 does not introduce saturation of the amplifier. Therefore output impedance does not strongly depend on phase of load VSWR.

As this amplifier behaves more or less linear, frequency difference method should give similar results. Result for frequency difference method, Vf.mimic = 9.47Vp (simulating phase varying VSWR=1.2), frequency difference 250 kHz, L=120.5nH - C=10pF series circuit added to avoid any DC shift and enhance harmonic suppression:

Zout = 7.1 + j15.2 Ohms (|RC| = 0.77 Arg(RC) = $+146^0$)

Increasing difference frequency to 500 kHz resulted in 7.0 + j16 Ohms.

This result isn't bad given the results from the load changing/pulling.

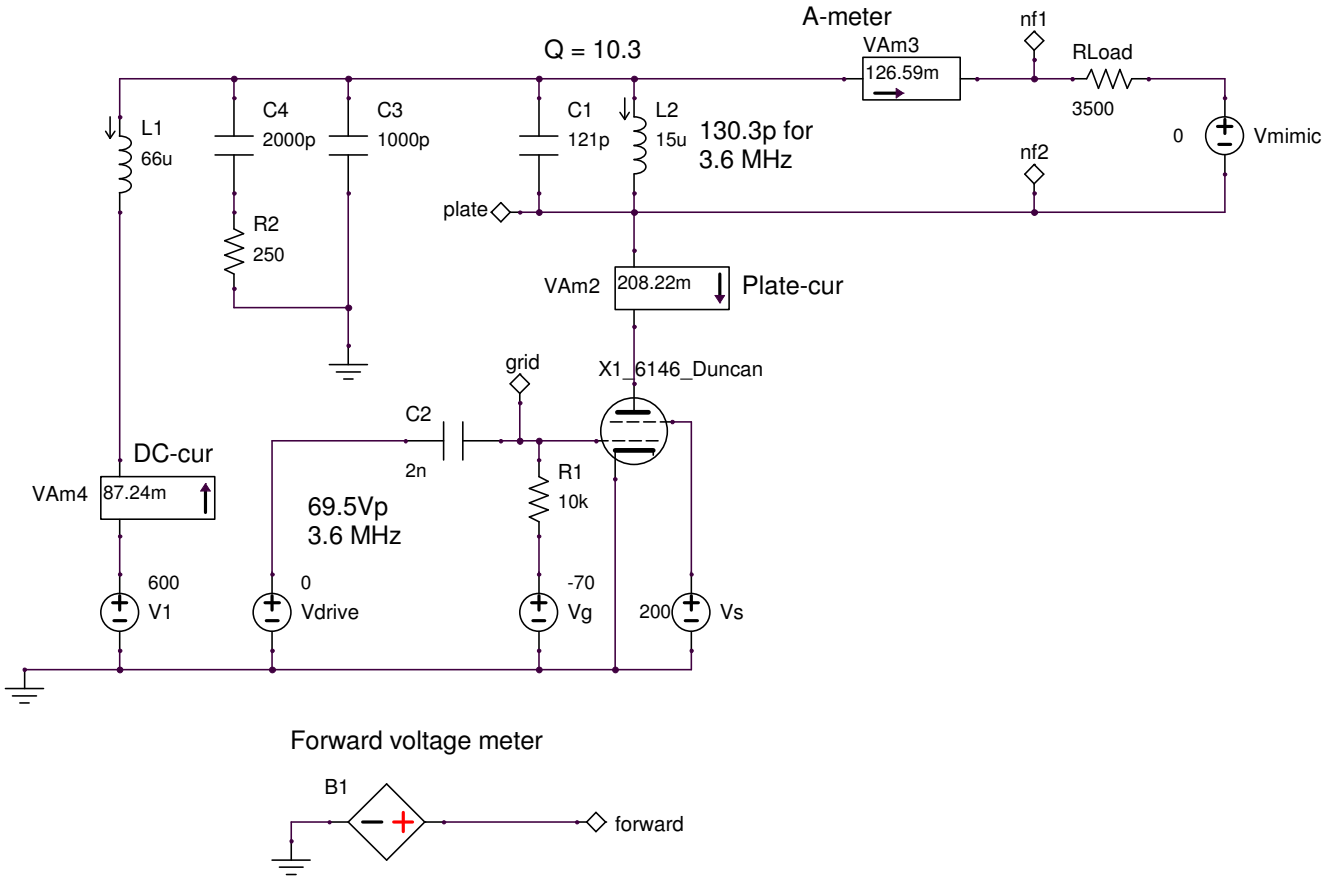
Real Class C amplifier in common cathode.

Goal of this circuit is to evaluate the output VSWR around saturation, circuit is kept very simple to ease reproduction.

The circuit is given below:

6146 class C amplifier, 3.6 MHz.

Class_C_amp_6146_CC1.ckt, Beige Bag Pspice A/D version 4.



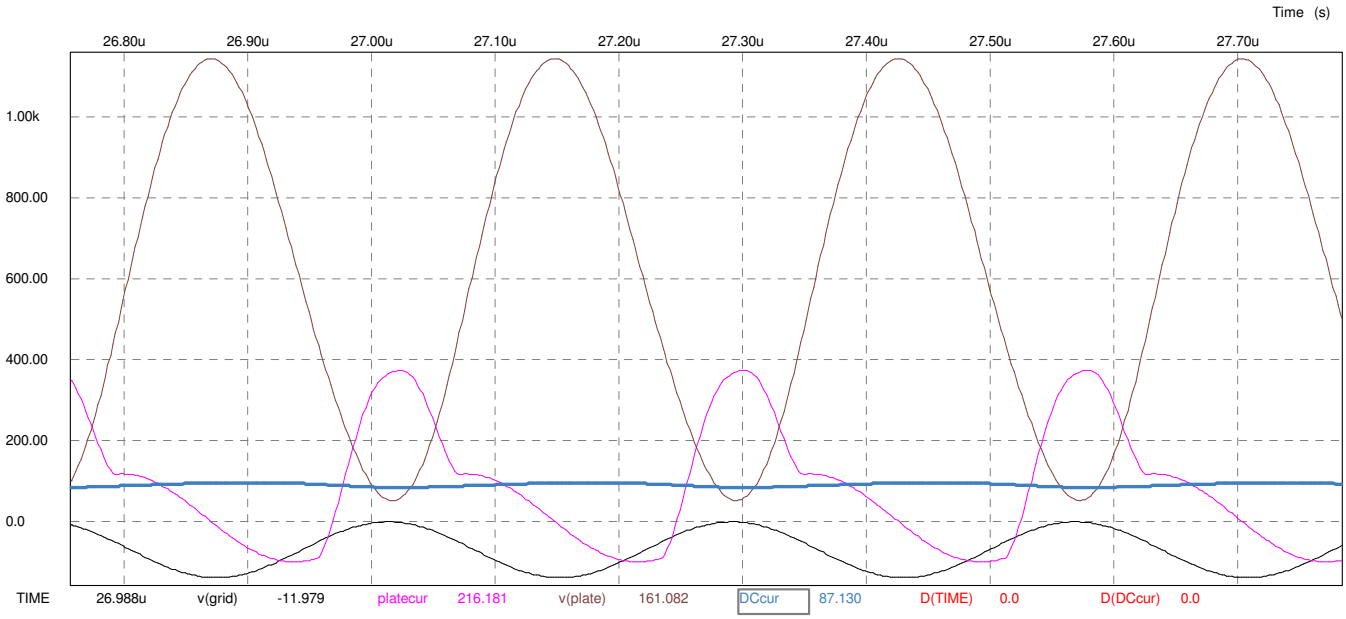
Forward voltage calculation for "forward" node
v = 0.5*(v(nf1) - v(nf2) + 3500*I(VAm3))

L1, C3, C4 is for filtering the supply current to enable current measurement. R2 is to reduce ringing when beginning the simulation. C2 has initial voltage of -70V to save simulation time (otherwise this capacitor must charge itself first).

The grid is driven from a voltage source to eliminate any plate to grid feedback via the Plate to Grid capacitance. Vmimic is zero.

RELTOL = 5u (0.005%), max step size = 2ns. Resistance to ground for analog nodes: 2 Gohm (HSPICE option). I have UIC option on, but this is not required if you are not interested in the start up behavior. .

Simulation results:



large black = plate voltage (1093Vpp)
purple = plate current (capacitive part can be clearly seen), mA, conduction angle = 140 degrees.
Thick blue is current through supply voltage, average value = 90.2mA
Small black (below zero) = Grid drive voltage.

Voltage drive is 69.5V. Vmimic = 0. Increasing the voltage leads to hard clipping. One can see that the peaks of the plate current are too rounded for a sine wave, so there is some saturation present. Tuning capacitor tuned for maximum efficiency.

Plate efficiency:

Input power = 600V*90.2mA = 54.12W
Output power = 0.5*(0.5*1093)^2/3500 = 42.67W.

Efficiency = 42.67/54.12 = 0.79 (79%).

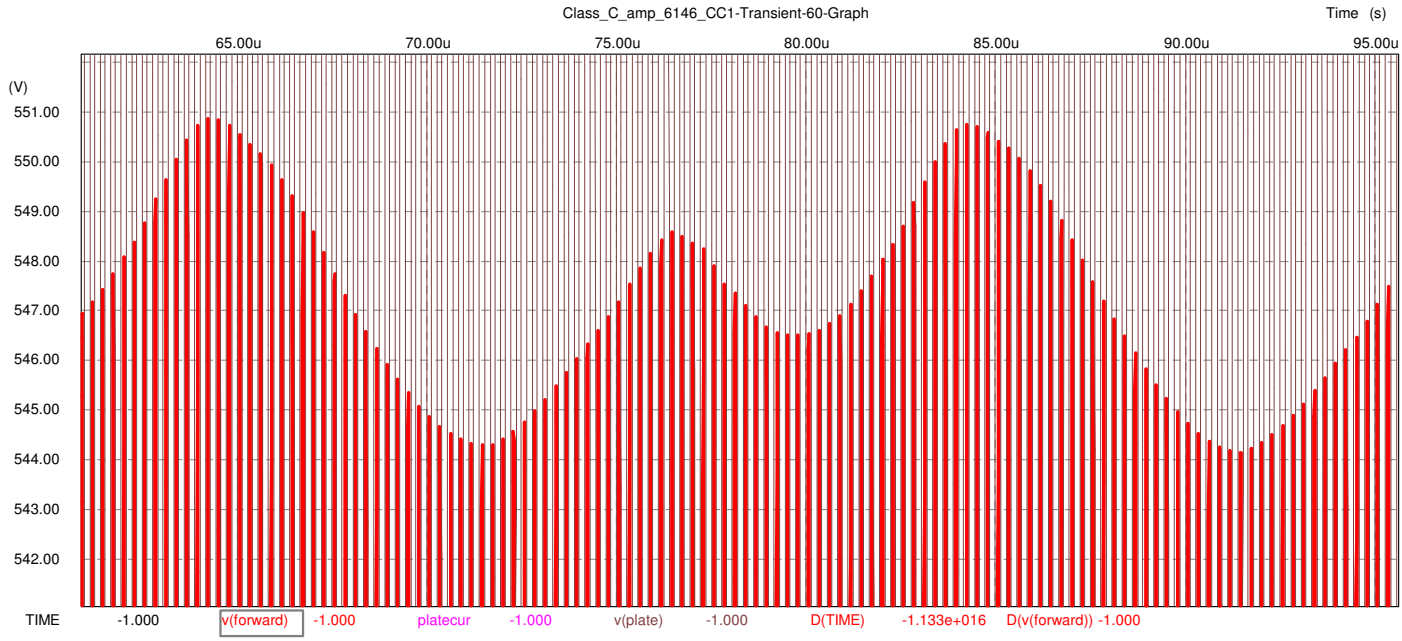
Output VSWR

Vmimic = 30Vp, 3.650 MHz, emulating a reflected voltage wave of 15V towards the amplifier. As the amplifier generate forward voltage of about 550V, the reflection coefficient (with moving phase) seen by the amplifier is

|RCout| = 15/550 = 0.0273 (load VSWR = 1.056, equivalent to 3696 and 3314 Ohms).

Because of the frequency difference of 50 kHz, it takes 20us to rotate the phase of reflection coefficient over 360 degrees. So maxima and minima in amplitude are 20us apart.

Below the largely zoomed output of the forward voltage is shown. This voltage is the sum of the forward voltage from the amplifier and the reflected 3650 MHz part.

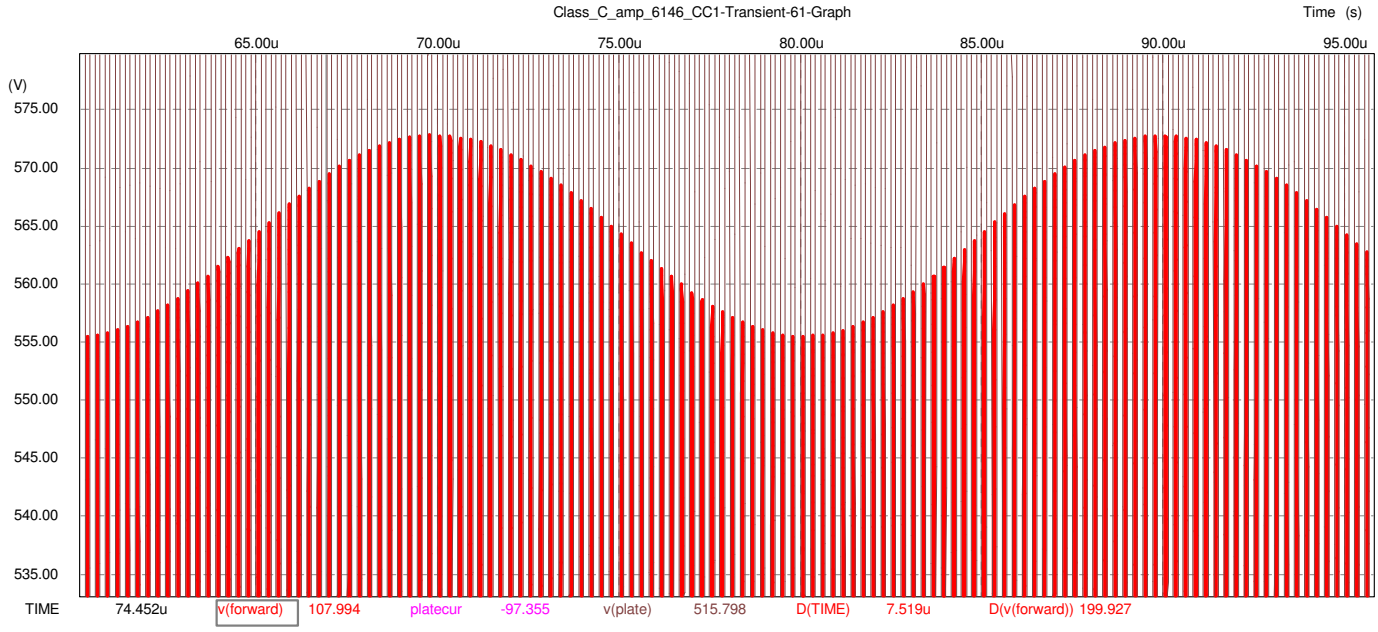


The envelope shows strong distortion, this is because of the valve is driven at the edge of saturation.

Vr.mimic = (550.9-544.2) = 3.35V.
Vf.mimic = 15V (half the EMF of Vmimic)

|RCout| = 3.45/15 = 0.22 (output VSWR = 1.58).

Increasing the excitation by 0.36 dB.
Now we change the driving voltage from 69.5 to 72.5V (that is increase of 0.36 dB).



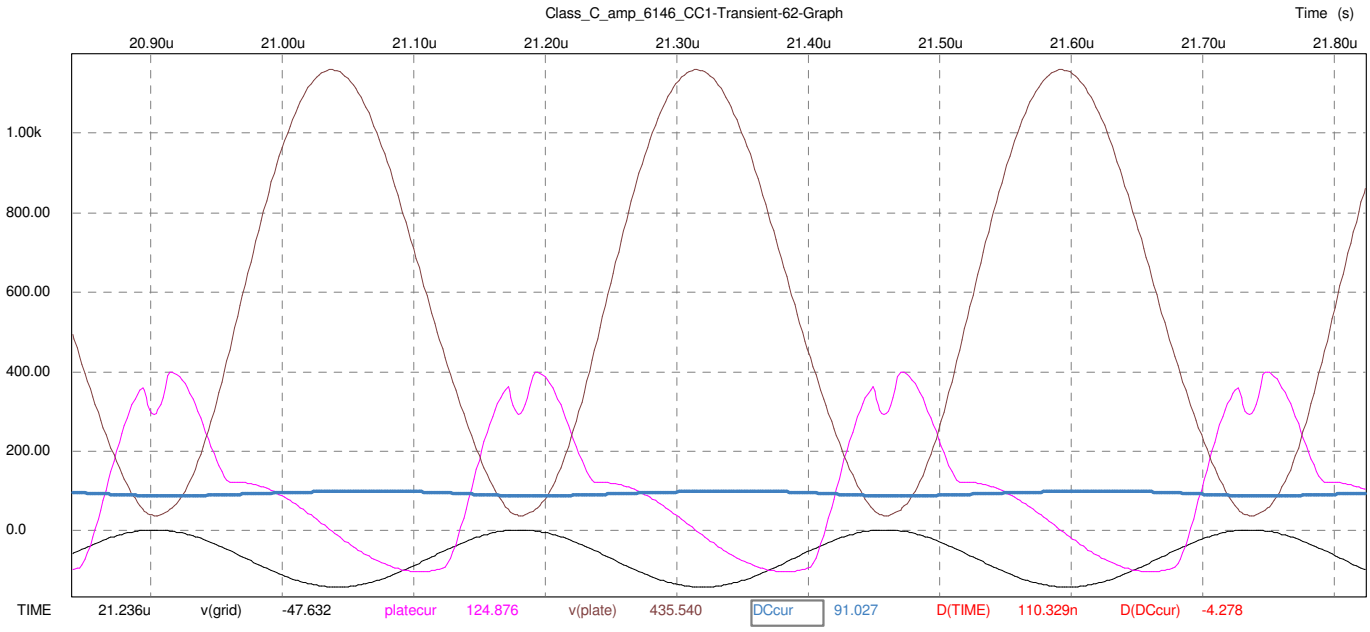
First one can see that the envelope is sinusoidal now, this because of over all phase angles, the valve remains slightly saturated.

Vr.mimic = (573-556)/2 = 8.5Vp.
Vf.mimic = 15Vp

|RCout| = 8.5/15 = 0.57 (output VSWR = 3.6, increased excitation).

Phase shift between envelope of load voltage and envelope of "forward" voltage is about 150 degrees (30 degrees off fully out of phase). So |Zout| will be below 3.5 kOhms, but not exactly real.

Below a detail of the plate current and voltage is given (with Vmimic = 0)



large black = plate voltage (1121Vpp)
purple = plate current (capacitive part can be clearly seen), mA, conduction angle = 145 degrees.
Thick blue is current through supply voltage, average value = 93.8 mA
Small black (below zero) = Grid drive voltage.

Efficiency

Input power = 600V*93.8mA = 56.28W
Output power = 0.5*(0.5*1121)^2/3500 = 44.88W.

Efficiency = 44.88/56.28 = 0.80 (80%).

Because the valve's saturation voltage of about 37V (for this amplifier), you lose about 6% efficiency (37/600 = 0.06), so the overall plate efficiency of 80% isn't bad.

Reduced excitation:
Results for driving voltage reduction from 69.5Vp to 66.5Vp:
Vr.mimic = 8V,
Vf.mimic = 15V. hence **Output VSWR = 2.88**.
Efficiency: 74%

Envelope of "forward" is almost in phase of envelope of load voltage, so 3.650 MHz reflected signal is almost in phase with the 3.650 MHz forward signal, hence output impedance is almost real 10 kOhms.

Further reducing the input voltage results in output VSWR > 5 (real output impedance > 17 kOhms.

Any doubts?, you can run the simulations yourself.

Conclusion on the output impedance of the real class C amplifier.
Though the efficiency of a real class C amplifier can be significantly above 50%, under very special circumstances the output impedance for very small load changes can be equal to the load resistor. This is of theoretical importance only.

The slightest change in load impedance or drive level results in significant changes to the amplifier's output impedance. Increase of drive results in reduction of output impedance, reducing the drive results in increase of output impedance. All values referenced to the plate of the valve where plate capacitance is cancelled via tank circuit.

Not proven here; when parasitic feedback is present, the impedance seen into the plate changes due to the feedback. The feedback capacitance to the plate results in increase of effective capacitance seen into the plate. You should not retune for this, as this reduces efficiency. So in a real amplifier you should look at both DC plate current and output power/voltage during tuning (as I learned from Jan, PA0AKS).

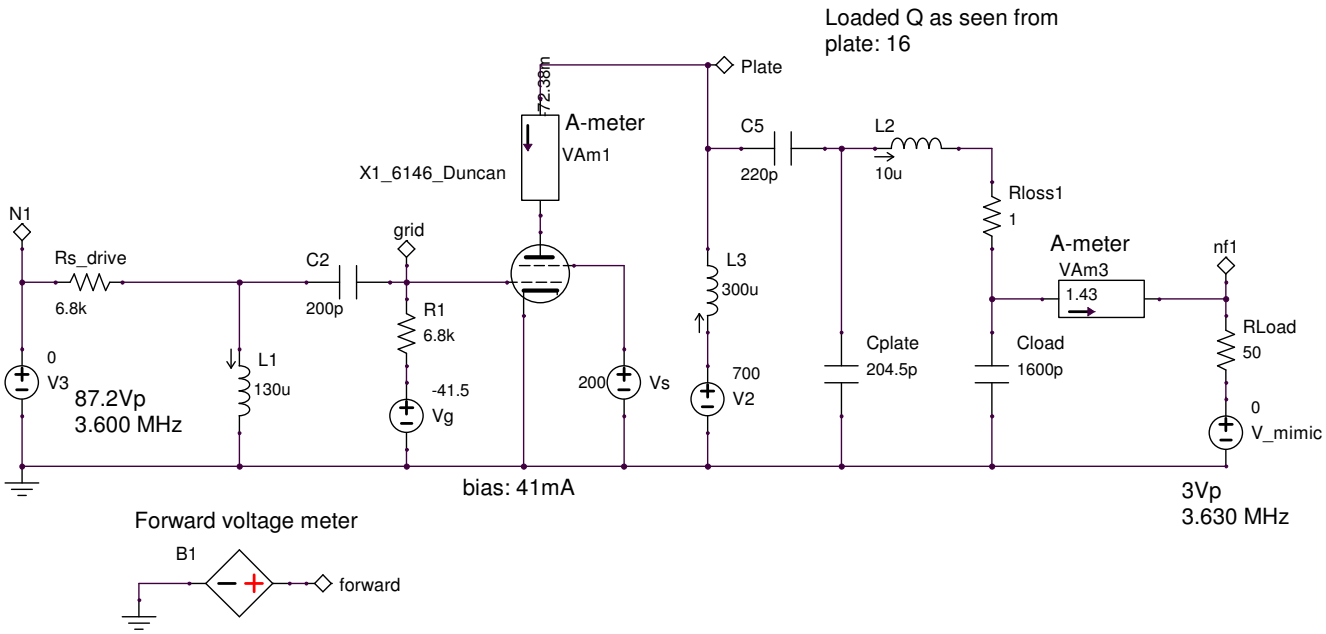
So practically spoken, there is no correlation between the efficiency of a class C amplifier and its output impedance. You can get almost everything you want.

Running simulation yourself? Make sure that increasing the accuracy and/or reducing "max step size" with about factor 2 doesn't change your results. If so, increase accuracy again and note difference with old results.

Single ended Class AB with pi-filter output network.

6146 class AB single-ended amplifier, 3.6 MHz.

6146ampCC_Pi_Filter4.ckt, Beige Bag Pspice A/D version 4.
transient simulation with reverse injection



Forward voltage calculation for "forward" node
v = -0.5*(v(nf1) + 50*I(VAm3))

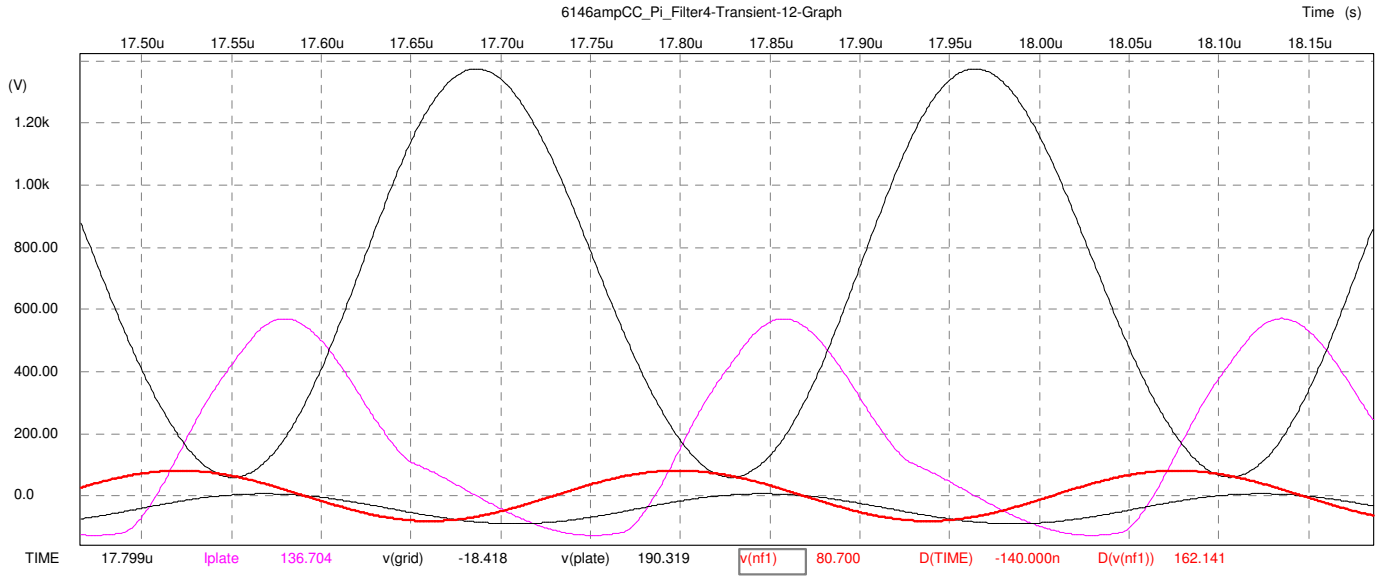
The Pi-filter transforms 3.490 kOhms to 50 Ohms with a Q=16 (seen from the plate), Excitation (V3) is 87.2Vp (EMF).

The drive circuitry is kept simple, but not a voltage source, as this eliminates the effect of the plate-grid capacitance. It is expected that output VSWR at reduced drive level depends on impedance of drive circuitry (seen from the grid).

The graph below (next page) gives relevant waveforms for the conjugated match case.

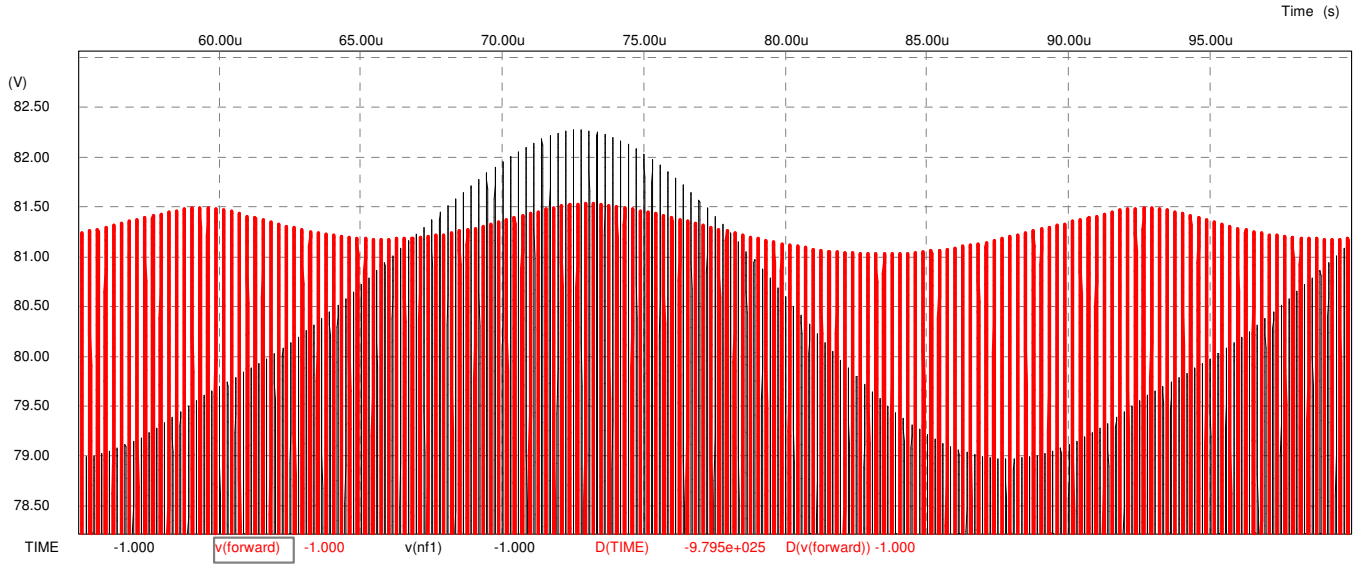
Output power = 65.7W
Input power = 700V*159mA = 111.3W
Efficiency = 65.7/111.3 = 59%.

Current through Rloss1 = 3.3Ap, this results in 5.4W heat loss (8% of output power).



Black = plate voltage (V)
Purple = plate current (mA)
Red = V(nf1) = output voltage into 50 Ohms, 162.1Vpp
Small black = grid voltage (V).
Average supply current: 159mA (not shown in graph)

Output VSWR under conjugated match condition.
Below relevant waveforms are given (Vmimic = 3Vp, 3.630 MHz):



Red = voltage at "forward"node: amplitude varies between 81.05 and 81.5V
Black = voltage at nf1

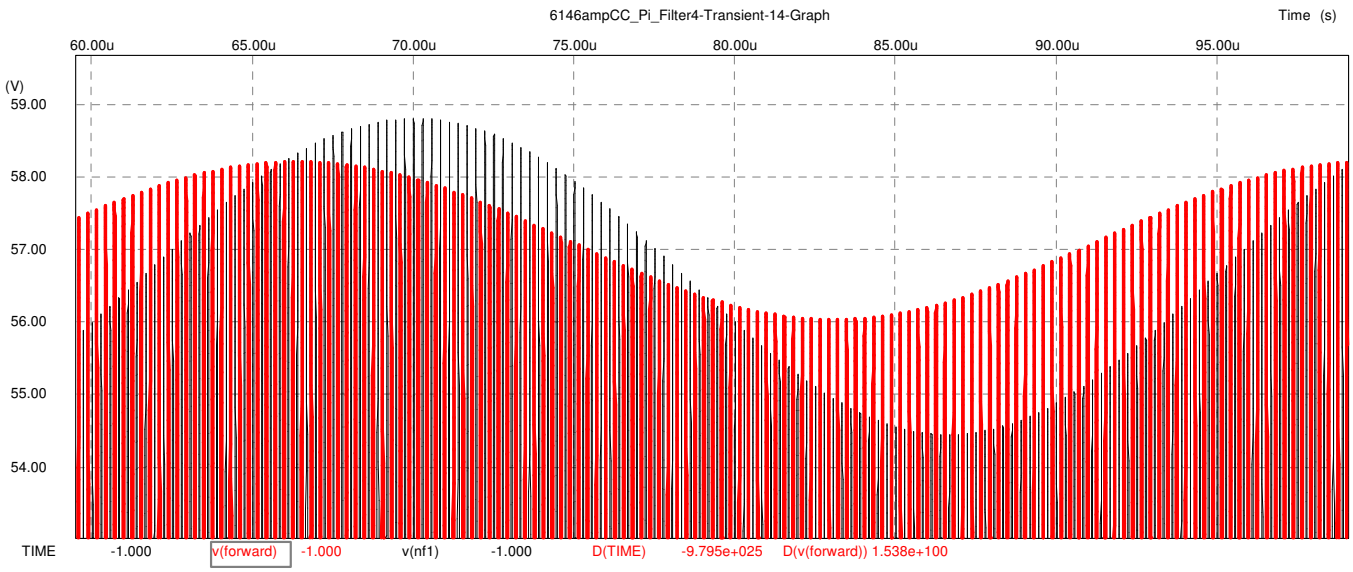
Vr.mimic = 0.23V,
Vf.mimic = 1.5V.
|RCout| = 0.23/1.5 = 0.15, (2.3% off maximum power),
output VSWR = 1.35 (37...68 Ohms)

In case of a linear system, the envelope of both red and black trace should be sinusoidal. Forward node envelope (red) is far from sinusoidal. This means that

the output impedance is non-linear (large change in Zout, for small change in operating conditions around the current operating point).

Output VSWR under reduced excitation.
Input drive is reduced with 3 dB from the conjugated matched situation discussed before (drive level = 62V).

Output power = 32.4W (3.07 dB reduction with 3 dB drive reduction)



Red = voltage from "forward", amplitude varies from 56.04 to 58.2V
Black = nf1 voltage, amplitude varies from 54.45 to 58.81
Peak of red envelope is 38 degrees in advance of black trace envelope

Vr.mimic = (58.2-56.04)/2 = 1.08 V,
Vf.mimic = 1.5V.
|RCout| = 1.08/1.5 = 0.72,
output VSWR = 6.1 (8.2...305 Ohms), 3 dB drive reduction

Envelope of black trace represents vector sum of forward wave (1.5Vp, 3.63 MHz) and reflected wave from amplifier (1.08V, 3.63 MHz).
Total voltage (sum) = 2.18V, 3.63 MHz. Due to the interference with the output wave from the amplifier, all voltages show as 30 kHz envelope.

From calculation: reverse voltage is 64 degrees in advance of forward voltage, so phase of reflection coefficient = +64 degrees, this correspondents to

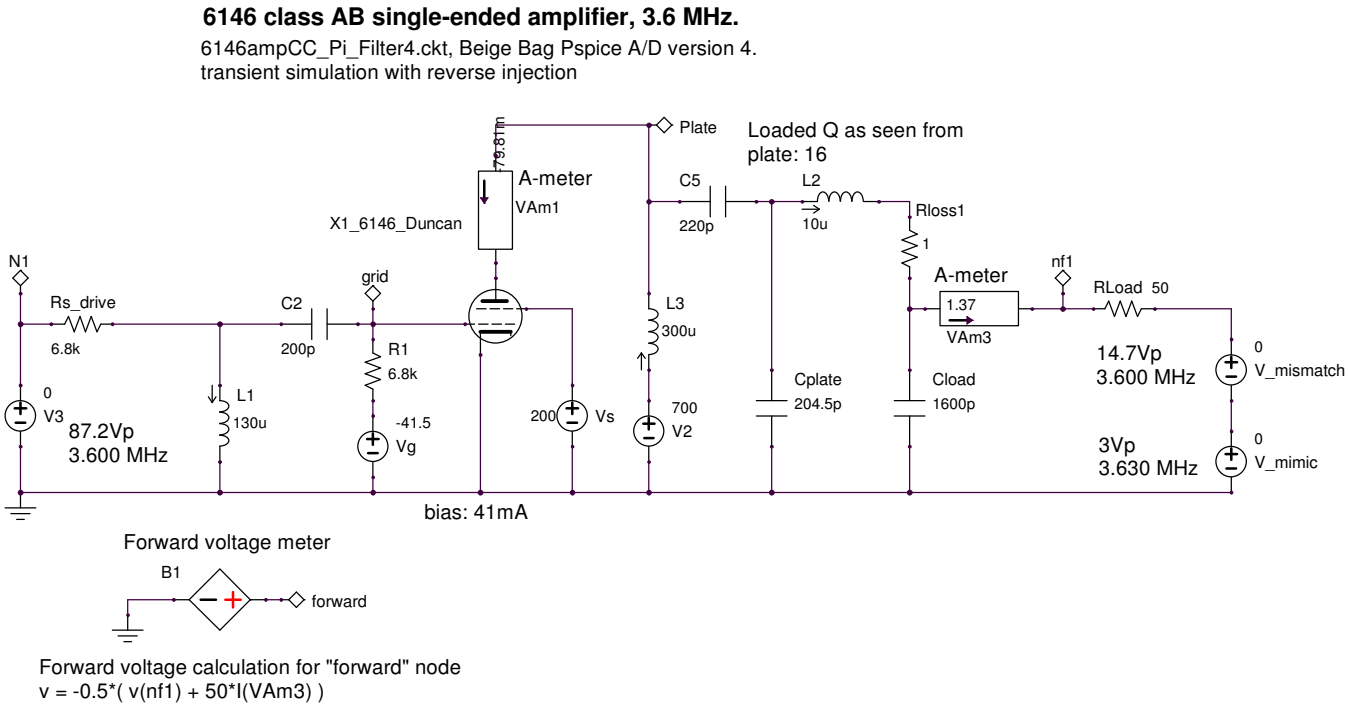
Zout = (27 + j73) Ohms.

As the output impedance is no longer real, a load pull with a resistive load directly connected to the amplifier will not give useful results, unless phase is included also..

In case of lossless Pi-filter, VSWR = 6.1 at plate, referenced to 3.49 kOhm. The actual VSWR will be somewhat higher because of 8% loss in the Pi-filter, but this is ignored. VSWR=6.1 referenced to 3.49 kOhms results in a parallel equivalent resistance of 570, or 21 kOhms. As we did the measurement for under drive, current source behavior dominates, so the valve appears to show 21 kOhms to the Pi-filter (of course with a parallel capacitance).

Output impedance under steady mismatch
Amplifier is adjusted as indicated in the circuit diagram; this is the conjugated match condition that resulted in low output VSWR (VSWR = 1.35) at about 66W output (at 87.2Vp EMF input [V3]).

The amplifier delivers a forward voltage of about 81Vp at 3.600 MHz into the 50 Ohms load. Now we add a source with 14.7Vp emf, 3.600 MHz (V_mismatch, synchronized with the driving voltage V3). This is often called "active load pulling". The additional source is shown in the circuit below:



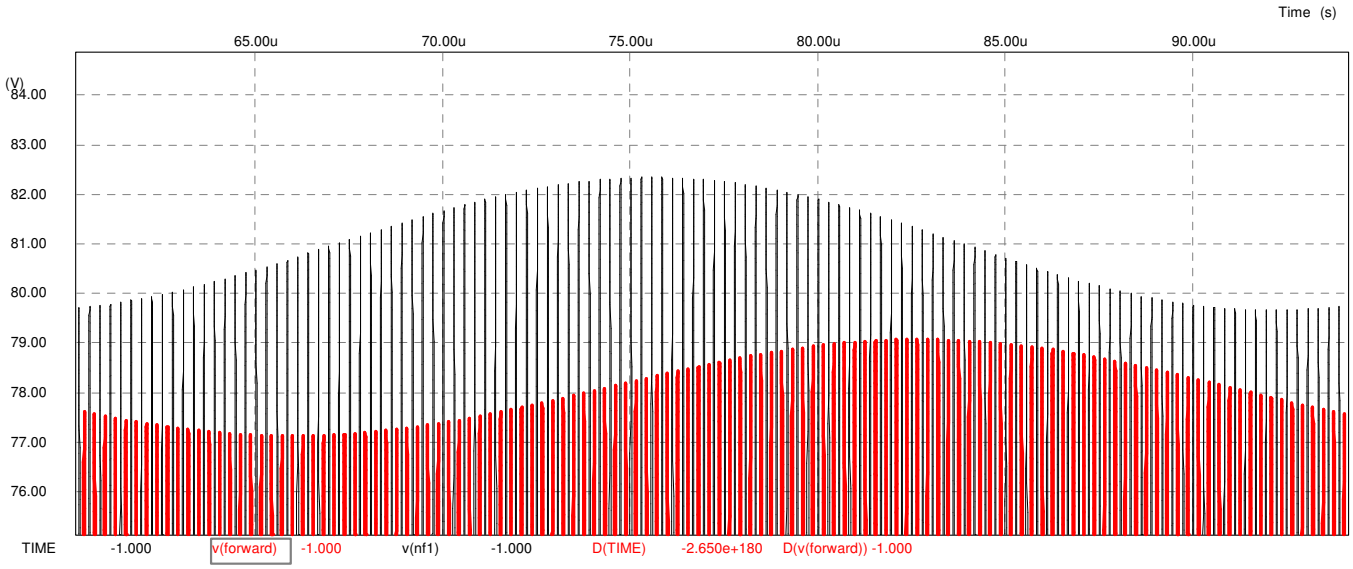
This results in a voltage wave towards the amplifier of 7.35Vp out of 50 Ohms This mimics a steady mismatch with

|RC| =7.35/81 = 0.091 (Load VSWR = 1.2, e.g. 60 or 42 Ohms)

By changing the phase of the voltage with respect to the input voltage, we can change the phase of the mismatch. The relative small reflection caused by this steady mismatch will not change the forward voltage generated by the amplifier (about 81Vp) significantly, so the error in the actual VSWR as seen by the amplifier will not be that large.

Vmimic (3Vp, 3.630 MHz) is used to measure the output reflection coefficient referenced to 50 Ohms.

Results for V_mismatch = 14.7Vp, in phase with V3.



Red = voltage at "forward" node: amplitude varies between 77.12 and 79.07V
Black = voltage at nf1

Vr.mimic = (79.07-77.12)/2 = 0.98 V,
Vf.mimic = 1.5V.
|RCout| = 0.98/1.5 = 0.65,
output VSWR = 4.8

Results for 4 different phase of VSWR = 1.2, |RC| = 0.091

Relative Phase change in VSWR [degr]	**Output VSWR (referenced to 50 Ohms) []**
0	4.8
+45	2.4
+180	3.8
+225	3.8

Power into load with VSWR = 1.5
Values derived from peak-peak output voltage simulations across real part of load impedance at 87.2Vp drive. Matching components remaining same.

Power into 50 Ohm (conjugated match):	65.7W	(=100%)
Power into 75 Ohms:	58.2W	(-11.4%)
Power into 33.3 Ohms:	65.0W	(-1.1%)
Power into 46.2-j19 Ohms:	52.1W	(-20.7%)
Power into 46.2+j19 Ohms:	50.6W	(-23.0%)

Power drop for VSWR=1.5 would be 4% assuming 50 Ohms load independent output impedance. The large variation in power loss versus phase angle cannot be justified because of output impedance (at conjugated match) isn't exactly 50 Ohms. This is because all loads with VSWR=1.5 result in power reduction, so actual output impedance is well within the VSWR = 1.5 circle.

Output impedance at conjugated match is likely to be somewhat below 50 Ohms, as 33.3 Ohms load gives less loss then expected for VSWR=1.5.

Load change/pull under 3dB reduced drive:
Load changed with 61Vp excitation (V3):

45 Ohms: Vout (nf1) = 53.1Vp, zero crossing at: 50.0921us
55 Ohms: Vout (nf1) = 57.8Vp, zero crossing at: 50.0885us
phase difference = +4.67 degrees.

Zout = 7.9 + j41 Ohm (VSWR = 10.7)

40 Ohms: Vout (nf1) = 50.2Vp, zero crossing at: 50.0940us
60 Ohms: Vout (nf1) = 59.7Vp, zero crossing at: 50.0871us
phase difference = +8.94 degrees.

Zout = 9.7 + j40 Ohm (VSWR = 8.5)

It is unknown whether the (relative small) difference is caused by simulation accuracy or non-linear behavior of the tube.

What can be concluded?
Output impedance is very sensitive to both change in drive level as well as load change. The root cause is that changing the drive level and/or changing the load, changes the amount of voltage saturation of the valve. This is not different from the other 3 valve amplifier examples.

Paralleling two valves (as present in various amateur HF transceivers) would reduce the mismatch at reduced excitation, however paralleling two tubes to get double output (that means changing output matching), will virtually not change the output VSWR.

Single ended Class AB PA with Pi-filter output network, but with low output power under conjugated match and special drive circuit impedance.

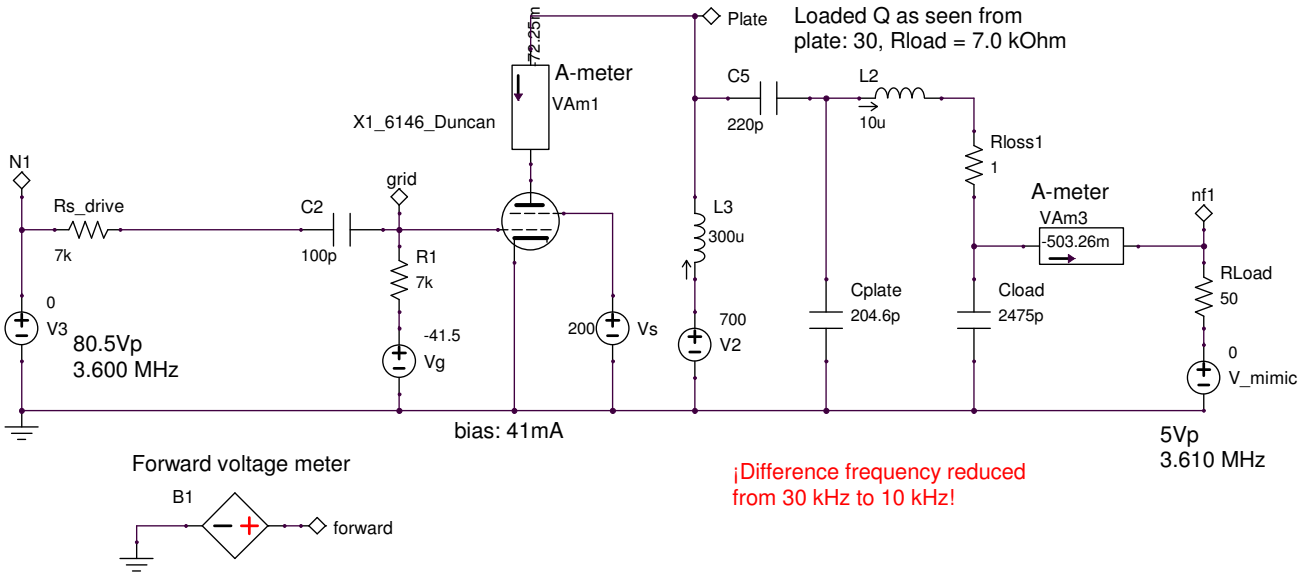
Is it possible to make a power amplifier that show 50 Ohms output impedance under reduced drive and varying load? Yes, within some limitations this is possible.

3 July 2010, Circuit retuned with 3.610 MHz phase changing VSWR signal (V_mimic) to be well within the bandwidth of the amplifier as using 3.630 MHz was too far from the center frequency.

An example circuit is given below. It looks almost similar as the one from the previous example, but the output circuit has changed (to get conjugated match under less power) AND the input drive circuitry has changed (to modify the valve's output impedance by changing the feedback via Cpg).

6146 class AB single-ended amplifier, 3.6 MHz.

6146ampCC_Pi_Filter_DrCh3.ckt, Beige Bag Pspice A/D version 4.
transient simulation with reverse injection

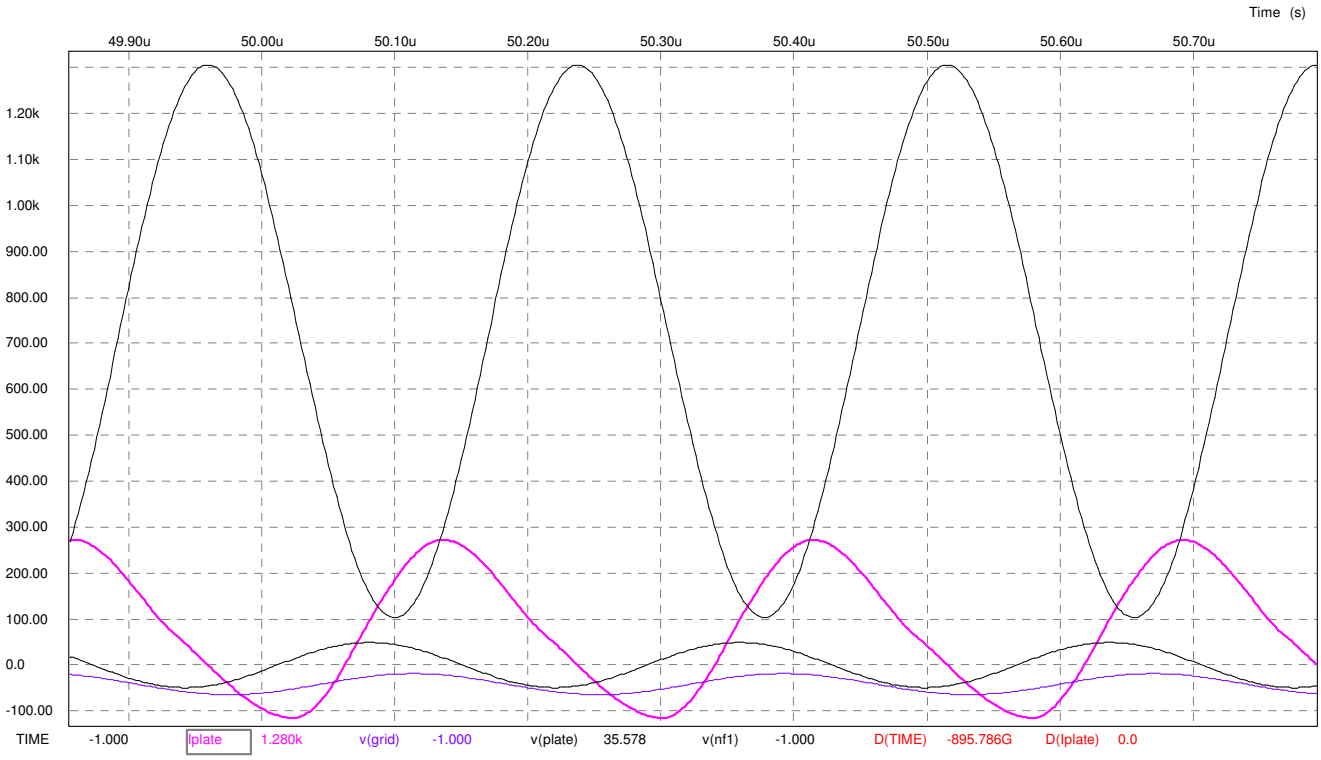


Forward voltage calculation for "forward" node
v = -0.5*(v(nf1) + 50*I(VAm3))

For important waveforms, see next page.

Output voltage into 50 Ohms = 49.15V,
RF output power = 24.2 W.
DC input power = 72.1 mA*700 V = 50.5W
Efficiency = 24.2/50.5 = 0.48 (48%)

Important wave forms (V_mimic = 0Vp):

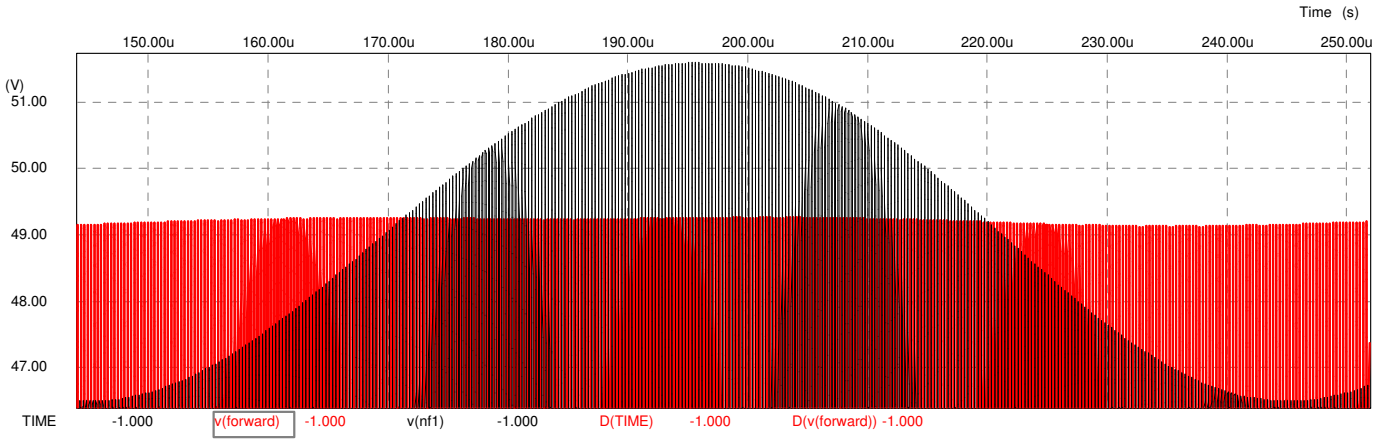


large black = plate voltage (V)
purple = plate current (mA)
blue = grid voltage
small black = V(nf1) = voltage across 50 Ohms (V).

Minimum plate voltage is about 104V, so far from the knee in the I_{plate} versus V_{plate} curve with V_{grid} as parameter and 50 Ohms load.

Output VSWR under conjugated match.
Pi-filter is tuned based on difference frequency method with V-mimic = 3.61 MHz. This method gives fast convergence to usable plate and load capacitor settings. Disadvantage is that you tune for 3.610 MHz, while the drive signal frequency is 3.600 MHz and pi-filter Q-factor is high. To show the effect of this, several measurements were done for both 3.60 MHz and 3.61 MHz.

All voltages are as indicated in the circuit picture. Below a magnified version of the "forward" voltage and V(nf1) is given (the artifacts are from dot joining (screen aliasing)):



Red = voltage from "forward", amplitude varies from 49.13V to 49.26V
Black = nf1 voltage, amplitude varies from 46.50V to 51.58V

Vr.mimic = (49.26 – 49.13)/2 = 0.065 V,
Vf.mimic = 2.5V (3.61 MHz).
|RCout| = 0.065/2.5 = 0.026,
output VSWR = 1.05

The envelope of the reflected signal (red trace) is not sinusoidal, so the amplifier is close to saturation at some load VSWR phase angle.

When using load change (load pulling, including phase, 3.6 MHz drive):

42.5 Ohms: Vout (nf1) = 45.37Vp, zero crossing at: 55.15138us
60.0 Ohms: Vout (nf1) = 53.22Vp, zero crossing at: 55.15019us
phase difference = +1.54 degrees.

Zout = 42 + j13.4 Ohm (VSWR = 1.40)

When using load change (load pulling, including phase, 3.61 MHz drive):

42.5 Ohms: Vout (nf1) = 45.24Vp, zero crossing at: 55.28088us
60.0 Ohms: Vout (nf1) = 53.71Vp, zero crossing at: 55.28043us
phase difference = +0.58 degrees.

Zout = 50 + j5.9 Ohm (VSWR = 1.13)

This value is simulated as actual "measuring" frequency for difference frequency method is 3.61 MHz instead of 3.6 MHz. There is reasonable agreement with the difference frequency method.

When using load change (load pulling, including phase, 3.61 MHz, but with 31.7 Ohms and 35 Ohms to simulate VSWR=1.5):

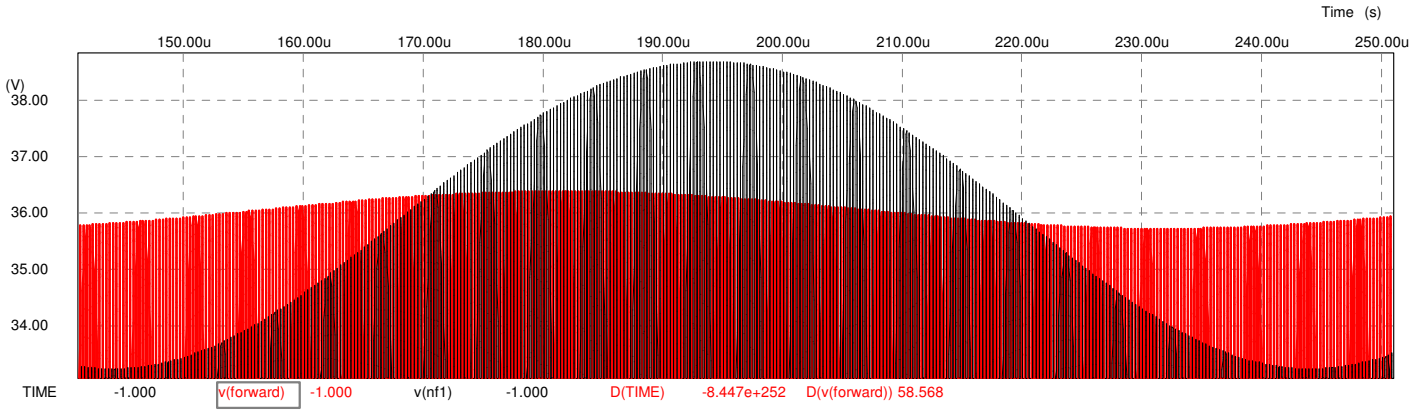
31.7 Ohms: Vout (nf1) = 37.85Vp, zero crossing at: 55.00427us
35.0 Ohms: Vout (nf1) = 40.30Vp, zero crossing at: 55.00425us
phase difference = +0.026 degrees.

Zout = 58 + j1.1 Ohm (VSWR = 1.16)

Load pulling with 71.4 Ohms and 78.8 Ohms at 3.61 MHz resulted in heavy plate saturation (plate voltage below 20V).

Zout = 22 + j8.5 Ohm (VSWR = 2.4)

Output VSWR under reduced drive.
Input drive (V3) is reduced from 80.5V to 56.9V (-3 dB).



Red = voltage from "forward", amplitude varies from 35.72V to 36.37V
Black = nf1 voltage, amplitude varies from 33.24V to 38.68V
Red trace envelope is12.34us (44 degr) in advance w.r.t. trace black envelope.

Vr.mimic = (36.37 - 35.72)/2 = 0.325 V,
Vf.mimic = 2.5V.
|RCout| = 0.325/2.5 = 0.13,
output VSWR = 1.30

Based on Reflection Coefficient (|RCout|) and phase between "forward" voltage and total load voltage envelope, output impedance of amplifier is:

Zout = 58 + j11.7 Ohm (VSWR = 1.30).

Output power into 50 Ohms is 13.0W (2.7 dB output power reduction for -3 dB input drive reduction).

When using load change (load pulling, including phase, 3.6 MHz drive):

42.5 Ohms: Vout (nf1) = 33.1Vp, zero crossing at: 55.15173us
60.0 Ohms: Vout (nf1) = 39.1Vp, zero crossing at: 55.15054us
phase difference = +1.54 degrees.

Zout = 45 + j14.5 Ohm (VSWR = 1.38)

When using load change (load pulling, including phase, 3.61 MHz drive):

42.5 Ohms: Vout (nf1) = 33.1Vp, zero crossing at: 55.15173us
60.0 Ohms: Vout (nf1) = 39.1Vp, zero crossing at: 55.15054us
phase difference = +1.54 degrees.

Zout = 59 + j5.9 Ohm (VSWR = 1.22)

This value was simulated, as actual "measuring" frequency for difference frequency method is 3.61 MHz instead of 3.6 MHz. There is good agreement with the result from the difference frequency method.

Conclusion regarding output impedance under varying load and excitation:
Yes, output impedance can maintain "conjugated matched" under varying load and excitation. Because hard power supply voltage, low difference frequency and relative small RF choke, results for difference frequency show reasonable agreement with load pulling. It is important to make sure the frequency used for frequency difference method is well within the pass band of the amplifier. Even 10 kHz off-center frequency changes results significantly (this is because of the high Q of the pi-filter). Therefore load pulling results are also shown for 3.61 MHz drive, giving better agreement.

Why is impedance relatively constant under varying load (as long as there is no saturation)? A simple analysis:
When matched, the plate sees a load resistance of 7 kOhms. This means that with plate voltage amplitude of about 600V and 700V supply, 24W can be delivered.

Feedback in electronics systems results in change of output impedance; this is widely used in electronic circuits to generate low impedance (voltage sources) and high impedance (current sources), but also to generate specific complex impedance. Feedback may result in negative output impedance as used in oscillators and active filters.

In this amplifier the plate to grid capacitance together with the output impedance of the drive circuitry (in this case 3.5 kOhms) is used to lower the output impedance of the valve to 7 kOhms. As long as there is no voltage saturation, the system behaves more or less linear. Drive setting is such that under normal operating conditions the plate voltage does not drop below 100V to avoid saturation. Increasing drive above 80.5Vp results in saturation, hence change in output impedance. Under this input drive level (80.5Vp), load VSWR = 1.5 (phase = 0^0) results in saturation, hence change in output impedance.

Can this special condition happen accidentally?
Yes, why not. It is more likely to happen when you use a device far below its intended power rating. To make it easier in simulation, output is reduced from 65.7W to 24W. However, a slight change in phase of impedance seen from the grid raises the output impedance rapidly resulting in change in the PA's output impedance. You can do this yourself in simulation by adding an inductor (or capacitor) and retune for conjugated match.

When using neutralization, or common grid circuit, the feedback is reduced on purpose. Therefore the output impedance of the device (non-saturating) is mostly above the load impedance that is required to deliver certain amount of power. This is especially true for solid-state devices (BJT, VDMOS and LDMOS transistors). So for conjugated match, you need (some) voltage saturation to get the large signal output impedance equal to Zload* ("*" means conjugated value). This is a strong non-linear process, hence changing drive or load, results in change of output impedance as is demonstrated in the simulations.

Note that under conjugated match and capacitive feedback, mostly charge carrier plate/drain current (ignoring the capacitive component) does not have optimum phase with respect to plate/drain voltage, hence reducing efficiency. As for the tube case low frequencies are used, the effect is not important here.

General notes on measurements/simulations.

1. Soft power supply voltage.
Here the simulations were done with hard supply. In case of a soft supply (limited DC power available), the matching for maximum output given certain input drive, may be more to a state with higher efficiency for some designs. This is because of change in power consumption will change supply voltage. This may result in a complex output impedance (some parallel capacitance present), that reduces |Zout|. When one would do the simulation based on the difference frequency, decoupling capacitors will make the supply hard, so you may get (slightly) different results, even at tens of Hz difference frequency.

Under manual load changing/pulling, bias voltages/currents (gate, screen, grid, base current) may find a new steady state. When using difference frequency method, decoupling capacitors in bias circuits may impede voltage changes. Therefore difference frequency (VSA) measurement results may differ from manual load change measurement results. Note that in the simulations hard bias voltages are used.

2. Chokes.
With load change simulations/measurements, current through chokes will settle. However with the difference frequency method, current may not settle. It can be seen that during the simulations with Vmimic, the DC current through the choke changes with the difference frequency. A large choke in combination with higher difference frequency would result in (slightly) different results. When using below kHz frequencies in a real measurement, the chokes will not be important.

2. Ideal components.
The components used in the simulation are ideal. In real world there will be loss, so VSWR will reduce somewhat. If you like, you can add loss resistances. This may be necessary if your simulation stops with a "time step too small" error or when is runs slowly. You will definitely run into such issues when simulating high efficiency designs where intended or parasitic PN junction conduction occurs.

Overall conclusion and extrapolation.

Under maximum power output matching given certain drive (not necessarily being the maximum drive), the output impedance equals the load resistor (the so-called "conjugated match condition").

As soon as one deviate from this, this will no longer hold, and the impedance shown to the plate/drain/collector is no longer equal to the impedance seen into the plate/drain/collector/etc. Here "deviation" means: changing load without retuning to maximum output or reducing the drive (without retuning to maximum output). When you want Zout = Rload under "deviation", you specially need to design for that (see second Pi-filter amplifier with 6146 valve).

Under SSB mode, a linear amplifier is not driven at the power obtained just after matching. This will result in change in output impedance (and this is no problem as long as the output remains clean).

Many amplifiers do not have easy accessible matching (single band amplifiers, push-pull wide band amplifiers [with ferrite transformers], narrow band push-pull amplifiers [transmission line baluns/transformers], etc), so it is unlikely that they are operated under conjugated match at all usable frequency and varying power levels.

Different measuring methods may result in different measurement results that cannot be explained by error analysis. Amplifiers may respond differently to static mismatch versus dynamically changing mismatch, mostly caused by power supply and bias supply filtering.

Maximum gain mostly doesn’t coincide with maximum efficiency; so several amplifiers are not operated under maximum output given certain drive. The IRF540N amplifier is such an example. Modern (semi) switching topologies (used by amateurs at the lower bands) provide high efficiency, but below the maximum gain that is attainable with the active device used. Externally tuning them for maximum power (given certain drive) will destroy them (like your audio amplifier at home when it has no protection). The 2m band linear amplifier is also not tuned to maximum output, but for reasonable efficiency under non-saturated conditions.

I hope these simulations encourage readers to do simulation themselves and develop an own opinion on the output impedance of RF power amplifiers. There are several free (for example LTSpice) or low priced PSPICE (Beige Bag) packages around that can be used for this purpose.

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Any comment is highly appreciated.

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